CBETA Beam Position Monitor System Design
And Plan for Measurement of Different Energy Bunches

R. Michnoff, J. Dobbins, R. Hulsart

October 2, 2018

CBETA Technical Note 030

Introduction

The purpose of this document is to describe the overall CBETA Beam Position Monitor (BPM) and Bunch Arrival Monitor (BAM) system architectures and define how the different energy accelerating and decelerating bunches will be measured. The CBETA machine layout is provided in figure 1.

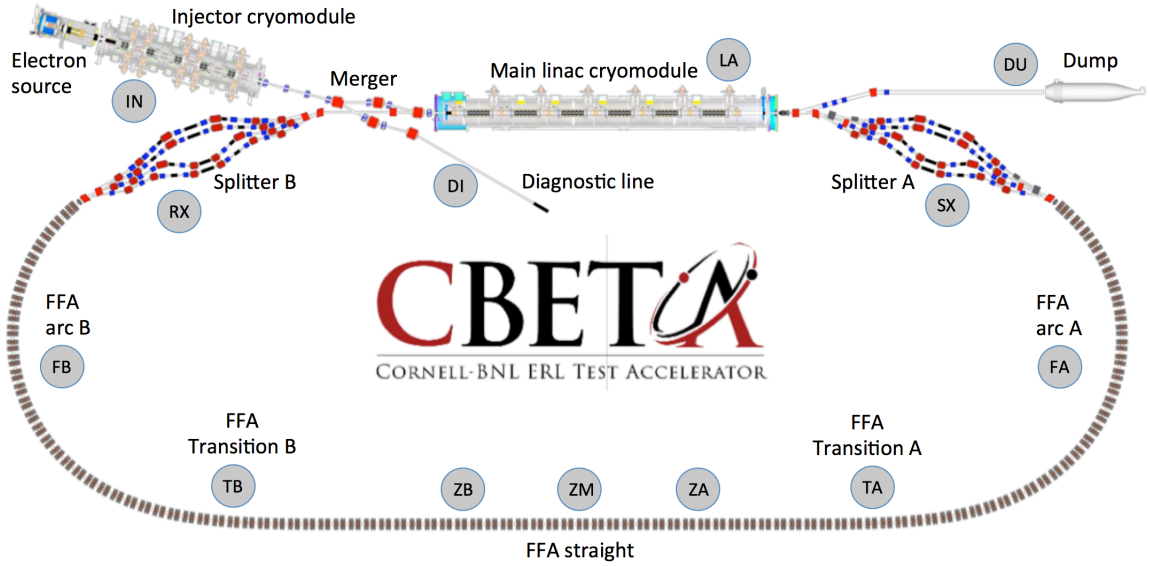


Figure 1. CBETA Machine Layout

Challenges for BPM Measurement

The major challenge for CBETA BPM measurements is that 7 different energy beams (4 accelerating and 3 decelerating) will be present in the FFA loop and must be independently measured; and BPMs at the entrance and exit of the main linac cryomodule (MLC) will need to independently measure 8 different energy beams. Additionally splitter lines 1, 2 and 3 will each include an accelerating and a decelerating beam with the same energy, which also must be independently measured.

BPM button chambers

Two styles of BPM button chambers are used for the CBETA splitter lines and FFA loop.

Photos of the round FFA loop BPM button chambers are shown in figure 2 and photos of the oval splitter line button chambers are shown in figure 3.

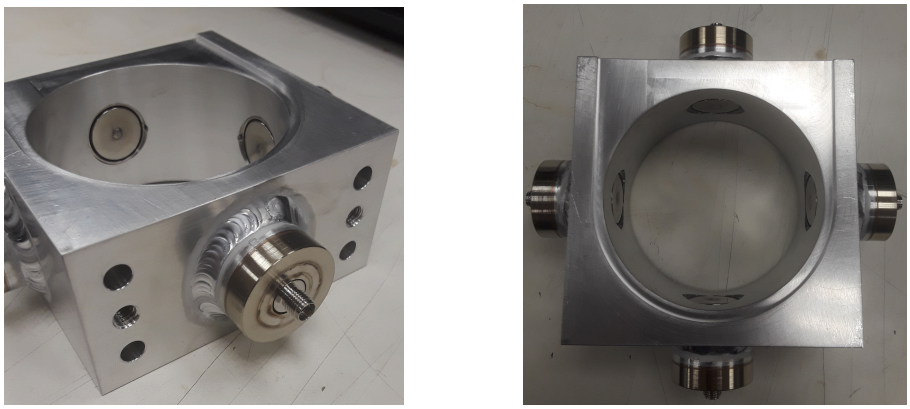


Fig 2. FFA loop BPM button chambers
Button diameter: 20 mm
BPM chamber diameter (FFA beam pipe diameter): 2.756 inches (70 mm)
Expected horizontal beam variations in FFAG: +/-24 mm

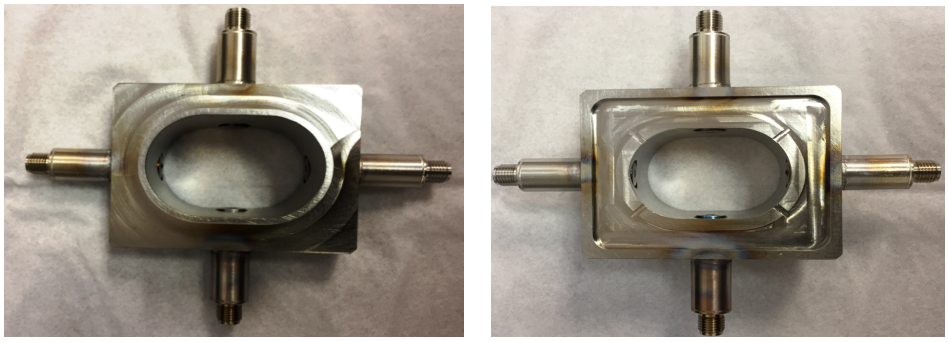


Fig 3. Splitter line BPM button chambers
Button diameter: 7 mm
BPM chamber diameter 36 mm (horizontal) x 24 mm (vertical)

Beam Position Monitors (BPMs) and Bunch Arrival Monitors (BAMs)

Most of the button signals will be used to measure position only (BPMs). These will be capable of independently measuring each of the energies in the beam pipe. Other button signals will be used to measure phase and position (BAMs) of bunch trains for a single energy beam only.

BPM/BAM Hardware Module

The CBETA BPM and BAM systems are based on the BNL designed V301 hardware module [1] (photo in figure 4) for front-end RF processing and data acquisition. A custom 500 MHz low-pass Bessel Filter was designed and installed on the board to limit ringing of the bunch signal, and significant custom firmware modifications are required to support the CBETA requirements.

Some of the V301 modules will be connected to a filter/mixer chassis for preprocessing of the V301 signals in order to provide position and phase measurements. These devices are referred to as Beam Arrival Monitors (BAMs).

Up to 15 V301 modules will be housed in each of about 12 total VME chassis. Each module provides a direct Ethernet connection to the higher-level control system. An EPICS IOC running under Linux will be resident on each V301 module for communication with higher-level software.

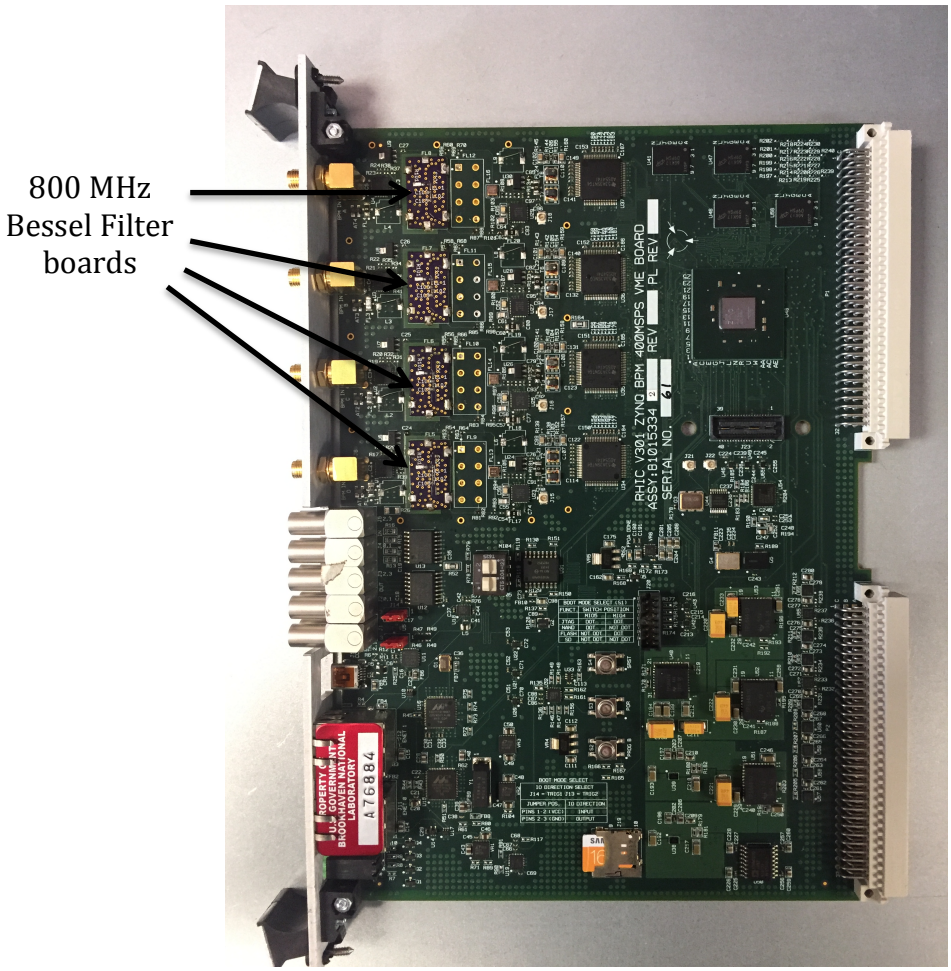


Figure 4. Photo of V301 module. Note custom Bessel low-pass filter board installed on footprint of original mini-circuits 500 MHz bandpass filter.

Beam Position Monitor (BPM) and Bunch Arrival Monitor (BAM) Hardware counts

The count of BPM chambers, BPM/BAM measurement channels, and electronic modules is provided in the table below.

Beamline section	**Number of BPM chambers**	**Number of BPM chambers connected to existing CU BPM/BAM modules**	**Number of BPM chambers connected to V301 modules for beam position measurement (BPMs)**	**Number of BPM chambers connected to V301 modules for position and phase measurement, bunch arrival monitors (BAMs)**
IN (injector)	5	5		
LA (main linac)	4 (3 in merger, 1 just after MLC)		4	1 (just before MLC, connected for very large bunch spacing mode)
SX (splitters)	20 (6 in S1 & S2, 4 in S3 & S4)		16	4
FFA (fixed field loop)	107		107	1 (first in FFA, connected for very large bunch spacing mode)
RX (splitters)	20 (6 in R1 & R2, 4 in R3 & R4)		16	4
DU (dump)	4		4	
DI (diagnostic)	4	4		
Total:		9	147	10
Total V301 modules rqd:			147	20 (2 V301 modules rqd for each BAM)

Table 1. BPM chamber and electronic module counts for each beamline section

For BAM measurements, the total quantity shown in the table assumes that two V301 modules are needed for each BAM. However, some may only require one V301 module. The measurements for S1, S2, S3, R1, R2, R3 will require 2 V301 modules each – one to measure the 1300 MHz filtered signals and the other to measure the 2600 MHz filtered signals. The 2600 MHz signals are used to measure the combination of accelerating and decelerating beams which are spaced by 180 degrees of 1300 MHz, thereby resulting in the measurable 2600 MHz signal.

Since the beam traveling through S4 and R4 includes accelerated beam only, then only 1300 MHz filtered channels are needed and therefore only one V301 module is likely required for each of these units.

The BAM measurements for the LA and FFA units may prove to be very difficult and if possible at all, will only be feasible in a diagnostic mode where a single bunch train is injected and allowed to be accelerated, decelerated and dumped before a new bunch train is injected. What makes this measurement difficult is that typically 3 or more 12.5 MHz periods (generated by a bunch train of about 15 bunches) are needed to obtain a valid phase measurement. Since the time for three 12.5 MHz periods is about 240 ns and the revolution time, or time between the different energy passes, is about 250 ns, the different energy signals may prove to be difficult to distinguish. (Ref. figure 25 for a BAM raw signal measurement during the fractional arc test with a bunch train of about 15 bunches.) A bunch train of fewer bunches may provide better separation of the signals, but will also sacrifice the accuracy of the phase measurement. Regardless, under normal operating conditions the LA and FFA units will be connected to a standard V301 module for beam position measurements only, and will be connected to BAM electronics only when dedicated diagnostics are desired.

BPM Acquisition technique

A single ADC sample on the peak of the selected energy bunch will be acquired for each of the 4 BPM button signals of the BPM for processing and position calculations. Many samples will be averaged in order to limit the sample-to-sample variations of the reported measurements.

In order to align the ADC sample to the peak of the selected energy bunch, the ADC clock will be locked to the RF clock. Therefore a stable clock is essential. This technique has already been tested and proven successful during the fractional arc test in April 2017.

Several configurable timing parameters are used to configure the V301 ADC clock to the peak of the selected energy bunch. With up to 8 different energy bunches needing to be measured by each V301 module, the timing parameters for each energy must be configured separately. It is not possible to use one common set of timing values to measure bunches of different energies. Table 2 in the "Bunch timing for each energy" section of this document provides details of the ADC clock timing variations for each energy.

Dedicated beam time will be required to configure the timing parameters for each of the energies. These timing settings will be stored within the EPICS IOC records. During normal operations the timing settings will be periodically changed to measure each of the different energies.

The procedure for automatically sequencing through the measurement of all the energy beams is as follows:

1. Set the timing values for energy 1 (This will require a few milliseconds of time to make the change)
2. Acquire n pilot bunch measurements at energy 1 (For about 10 ms of acquisition and a pilot bunch injection every 8 turns, n = ~5000 (10ms / (262 ns per turn * 8 turns) = 4770)
3. Average all n measurements at energy 1
4. Change the timing values for energy 2 (This will require a few milliseconds of time to make the change. During this time, no measurements will be taken.)
5. Acquire n pilot bunch measurements at energy 2
6. Average all n measurements at energy 2
7. Continue this sequence for all the energies to be measured.
8. Deliver the average data for all the energies measured.

A diagram of the sequencing is shown below.

Set timing for Energy 1	Acquire n measurements for Energy 1, calc. avg	…	Set timing for Energy 8	Acquire n measurements for Energy 8, calc. avg	Deliver data for all energies

Using the example timing shown above, position measurements for all energies would be delivered about every 100 ms (10 Hz). However, the actual rates may need to change depending on testing after this concept is implemented in the hardware.

In addition, a position data array will be delivered at a maximum rate of every one-second. This array will be the concatenation of all of the energy bunches measured, including zeros for the dead time where the timing values are switched. The exact position data array size and time between samples is yet to be determined.

Hardware Architecture

As previously mentioned, up to 15 V301 modules will be installed in each of about 12 VME chassis. A photo of one fully populated VME chassis is provided in figure 5.

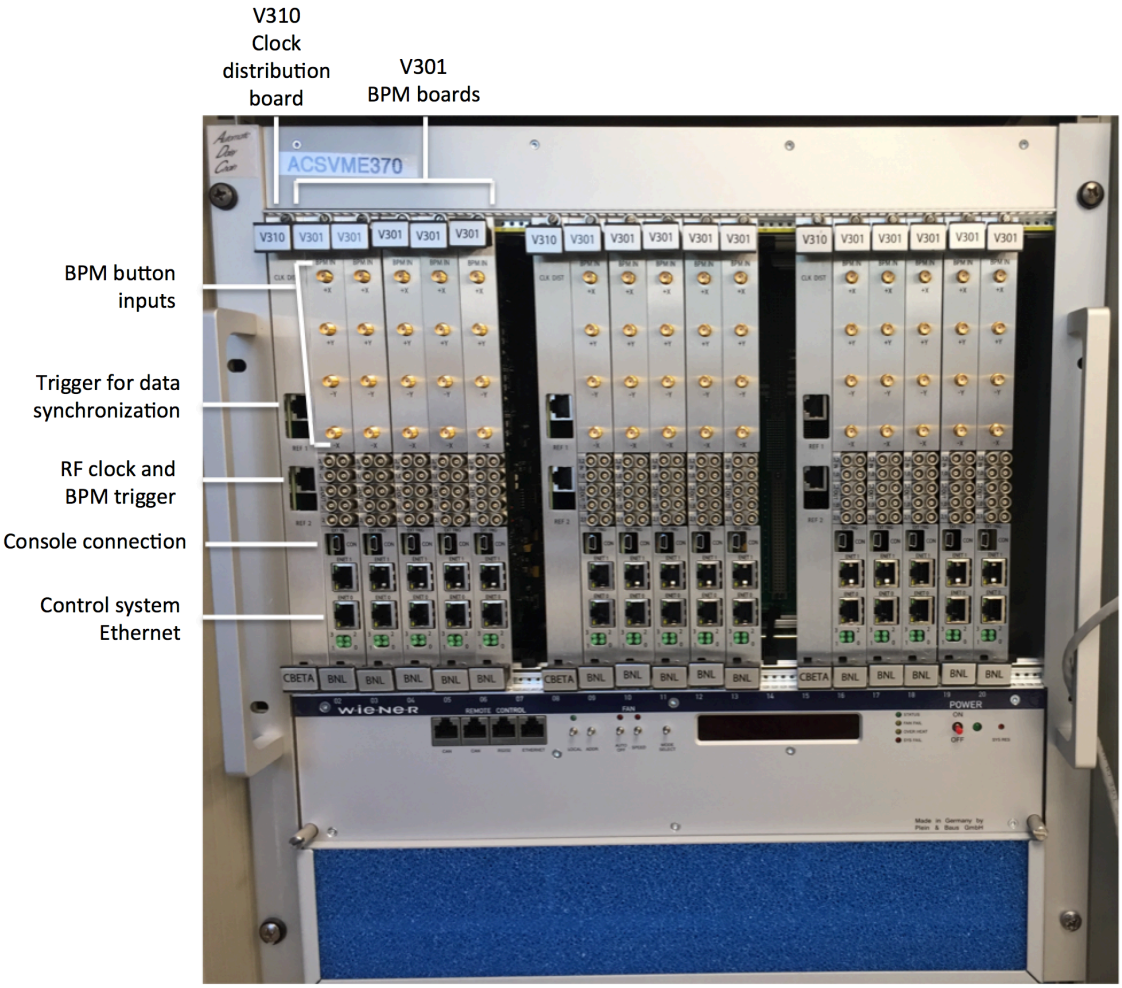


Figure 5. Photo of fully populated VME chassis with 3 sets of 1 clock distribution board (V310) and 5 Beam Position Monitor modules (V301). The four sma connectors on each V301 are for the 4 button signal inputs per BPM. The bottom RJ45 connector on each V301 (ENET2) is for control system Ethernet communication. The RJ45 Ref 2 signal on each V310 is for the RF clock and BPM trigger input, and the RJ45 Ref 1 signal on each V310 is for data synchronization triggers to the V301 modules.

A block diagram of the clock and trigger distribution is shown in figure 6.

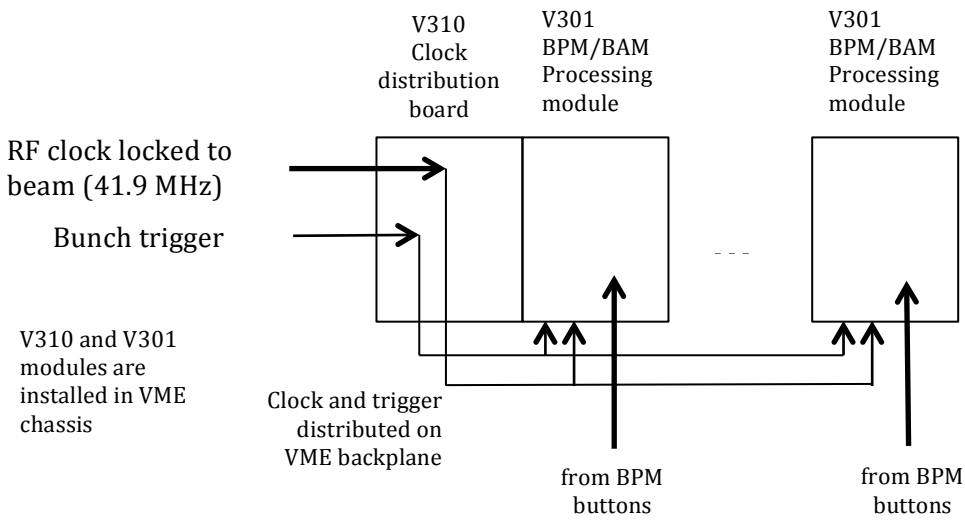


Figure 6. Block diagram of BPM and BAM module installation. An RF clock and bunch trigger are provided externally and connected to the V310 clock distribution module which distributes the signals to up to 5 V301 modules via an overlay backplane module. The data synchronization trigger is not shown on the diagram but will also be distributed similar to the RF clock and bunch trigger signals.

A block diagram of the analog signal chain for the CBETA V301 module is shown in figure 7.

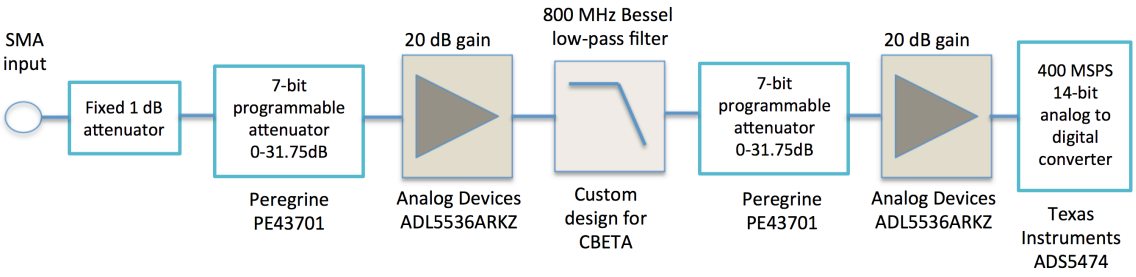


Figure 7. CBETA V301 BPM module analog signal chain (1 of 4 channels shown). Note the custom designed 800 MHz Bessel low-pass filter specifically for CBETA electron beam.

Beam Arrival Monitor (BAM) front end filter/mixer chassis

A block diagram of the filter/mixer chassis for bunch arrival monitor (BAM) phase measurements is provided in figure 8.

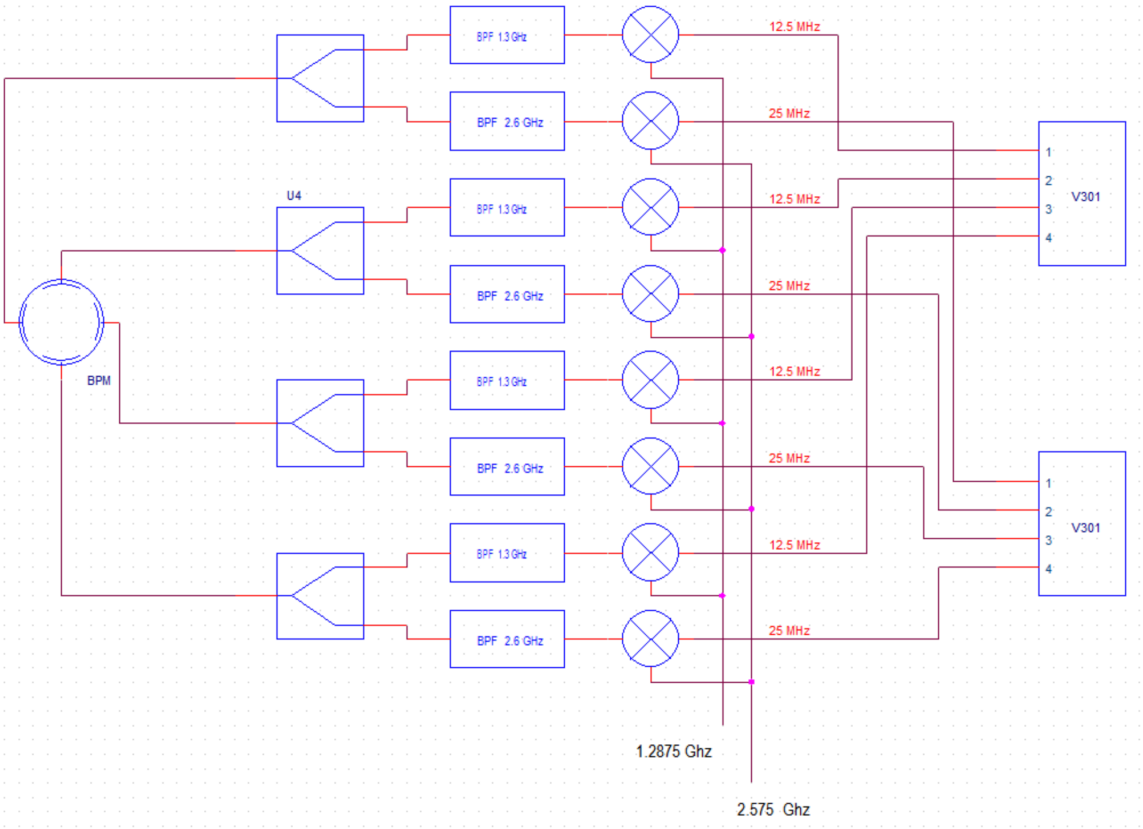


Figure 8. Block diagram of BAM filter/mixer chassis components.

Two V301 modules are planned to be used for each BAM – one for the 1300 MHz processing and the other for 2600 MHz processing.

The 2600 MHz signal will be used to measure the combination of the increasing and decreasing energy bunches as will be present in splitter lines 1,2 and 3. With 180 degree 1300 MHz spacing between the accelerating and decelerating beam, a 2600 MHz signal will be present for measurement. Only 150 MeV accelerating beam will be present in splitter line 4, so the 2600 MHz frequency module will not be required for the BAM in splitter line 4.

Bunch pattern and pilot bunches for BPM measurements

Figure 2.8.2 in the CBETA Design Report [2] (duplicated below) illustrates the bunch spacing within and between typical bunch trains. The spacing between the accelerating bunches and between the decelerating bunches is 2 1300 MHz RF periods or about 1.5 ns. This is insufficient spacing for the BPM electronics to distinguish between the different energy bunches. Therefore, a special pilot bunch train will be used specifically for BPM measurements.

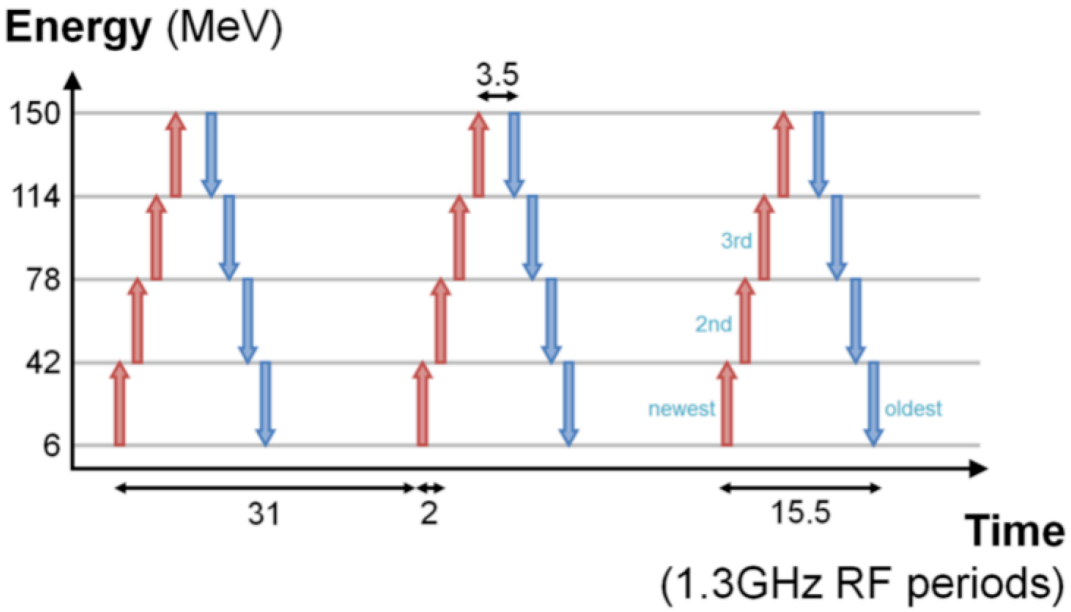


Figure 2.8.2: Bunch train details in the eRHIC-like mode. Note the top-energy bunches are well-separated (by 3.5 RF wavelengths).

Note: Since figure 2.8.2 was developed, the splitter line 4 path length has been changed, adding 1 additional 1300 MHz RF period. So the distance from the highest energy accelerating bunch to the highest energy decelerating bunch changes from 3.5 1300 MHz RF periods to 4.5 1300 MHz RF periods.

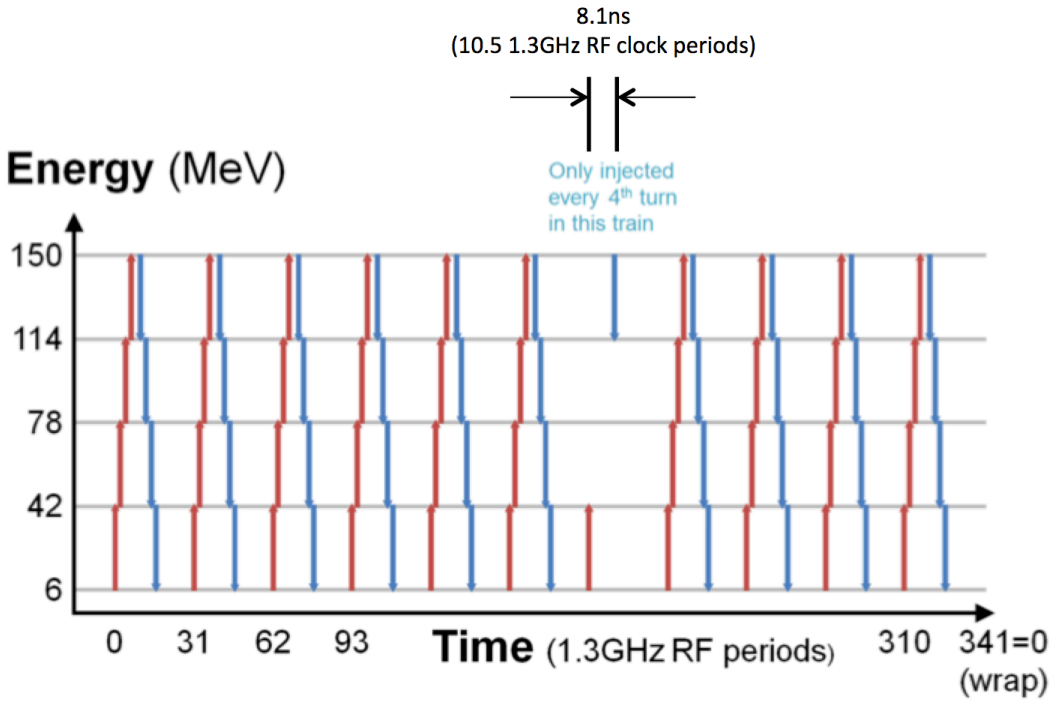


Figure 2.8.1: Bunch pattern produced in the eRHIC-like mode that has a circumference of $h = 343$ RF wavelengths but a time periodicity of 341 RF periods.

Figure 2.8.1 in the CBETA Design Report (duplicated above) illustrates a bunch pattern in the machine as seen at the Main Linac Cryomodule (MLC) for one complete revolution. The beginning of each line shows the energy upon beam entry into the MLC and the arrow end of each line shows the energy upon exit of the MLC. In order to accurately measure a single energy bunch, a minimum spacing of about 7 ns is required to ensure that interference between signals does not occur. In figure 2.8.1, note the 8.1 ns (10.5 1300 MHz clock periods) gap between the accelerating and decelerating bunches. These are the bunches that will be used for BPM measurements, and are referred to as the pilot bunches.

The typical injection rate is every 31 1300 MHz RF clocks. The gap is created by injecting one bunch every 4 turns for this pilot bunch train instead of every turn as is done for all the other bunch trains. The term "bunch train" is used here to mean one of the 11 groups of bunches in the full 343 1300 MHz RF wavelengths of the machine as shown in Figure 2.8.1. Ten of the eleven bunch trains include 8 different energies, while the pilot bunch train includes only 2 different energies. When the pilot bunch is injected every 4th turn, the pilot bunch train includes one accelerating bunch and one decelerating bunch, where each energy pair repeats every 4 turns. If the pilot bunch is injected every 8th turn which is another possible mode of operation, the pilot bunch train will include only one bunch – either an accelerating bunch or a decelerating bunch. This may provide a better BPM measurement of the decelerating bunch since an even larger time period will exist immediately preceding the decelerating bunch being measured.

RF locked ADC clock

For the fractional arc test, the RF clock frequency into the BPM system was 50 MHz. This was multiplied by 8 to generate a 400 MHz ADC clock.

For the full CBETA machine configuration, the RF clock frequency that will be used as input to the BPM system will be 41.935 MHz, which is the CBETA laser repetition rate (1300 MHZ RF / 31).

The revolution injection rate is therefore defined as follows:

revolution injection rate
= 1300 MHz RF frequency/31 rf clocks per train /11 trains per revolution
= 3.8123 MHz

An ADC clock close to the max rate of 400 MHz, which is optimal for the V301 hardware, will be used. This will be accomplished by programming the V301 PLL to multiply the 41.935 MHz clock by 38 and divide by 4 to get 398.387 MHz:

V301 ADC clock rate
= 41.935 * 38 = 1593.5 MHz / 4 = 398.387 MHz

The 1593.5 MHz frequency is the phase lock loop (PLL) frequency, which for the V301 hardware must be in the range of 1450-1800 MHz.

With this configuration the number of 398.387 MHz clocks does not fit evenly into a 41.935 MHz period (38/4=9.5), so only every other 41.935 MHz bunch can be timed to the peak (19 398.387 MHz clocks fit evenly into 2 41.935 MHz periods). This however is not expected to cause a problem. What is more important is that the number of 398.387 MHz clocks fit evenly into the injected pilot bunch period, which is every 4^{th} or 8^{th} turn.

Number of 398.387 MHz ADC clocks with pilot bunch injection every 4^{th} turn
= 38/4 * 11 injection buckets per turn * 4 turns
= 418

If pilot bunches were injected every turn (or on any odd number of n turns), measuring every injected pilot bunch would not be possible, but since the plan is to inject pilot bunches on an even number of turns (4 or 8), all is good.

Number of 398.387 MHz ADC clocks per revolution = 398.387/3.8123 = 104.5

Definition of V301 timing parameters

Figure 9 shows the ADC clock signal path and the programmable parameters for configuring the timing to the desired bunch.

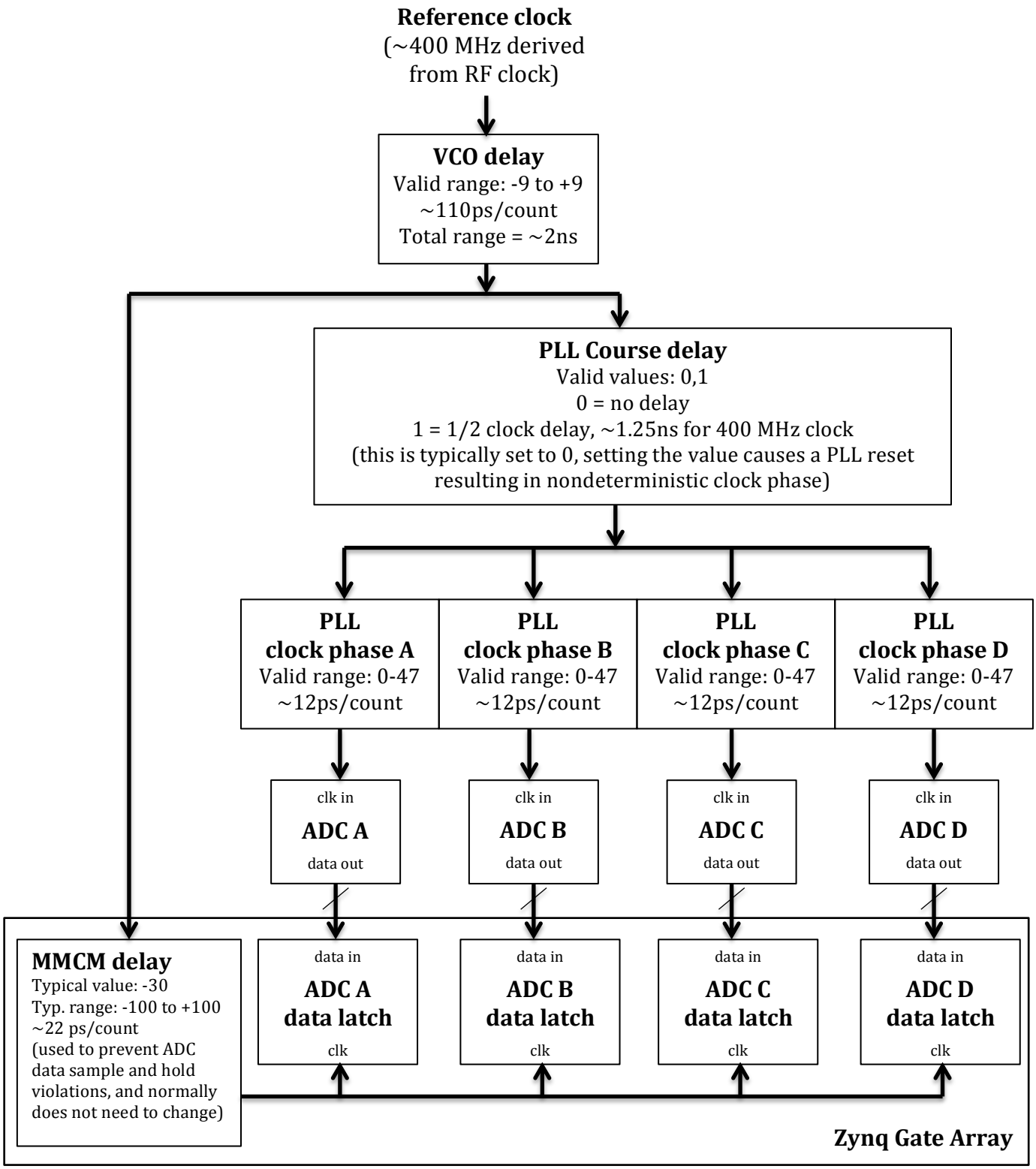


Figure 9 – V301 ADC clock delay parameters and signal flow diagram

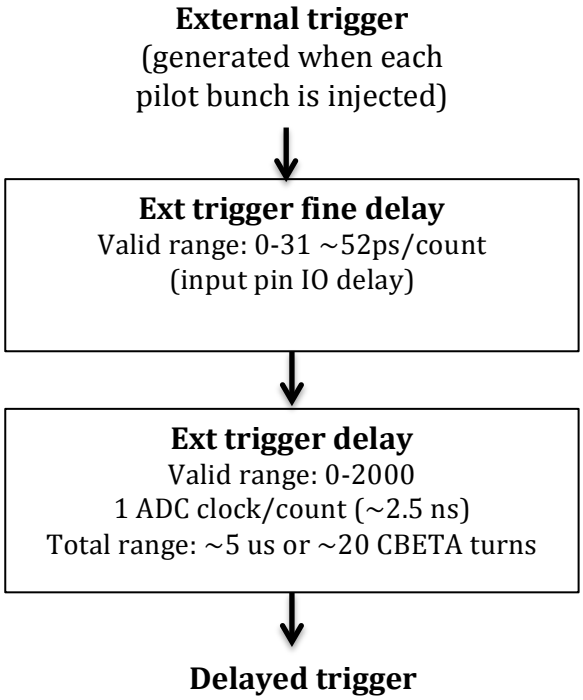


Figure 10 – V301 ADC External trigger delay parameters

The external trigger delay timing values are shown in figure 10. The external trigger fine delay is used to prevent signal jumps when doing profile scans. This is incremented automatically while the profile scan is performed. The value is normally set to 0, but in some cases can be changed to prevent a race condition between the external trigger and the gate array ADC clock. A race condition would cause the desired ADC data sample to jump between 2 clock edges.

The external trigger delay will be implemented in the V301 gate array code using a set of cascaded counters using the ADC clock as the counter clock. The anticipated counter configuration is shown in figure 11.

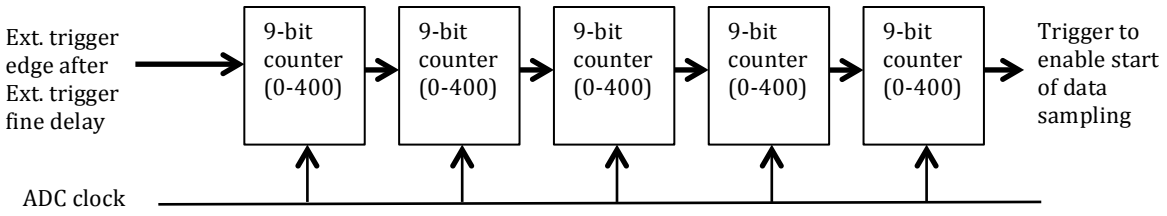


Figure 11. Cascaded trigger delay counters.

With this configuration, a total delay of 2000 ADC clocks is possible, resulting in just under 20 turns. Each counter's upper limit is defined to be 400 or just under 4 turns (Number of ADC clocks in 4 turns = 9.5 ADC clocks per injection period * 11

possible injections per turn * 4 turns = 418). Assuming that the BPM pilot bunch triggers will not be generated more than once every 4 turns, this limit of 400 will allow a new external trigger to propagate into the first and subsequent counter stages without loss of any external triggers. If any of the counters are set to 0, the input to output must propagate directly to prevent minimum delays of 1 count for each counter.

Bunch timing for each energy

Table 2 shows the delay times required to measure a bunch at each energy. The delay times shown are referenced from the first turn for BPMs having a first pass energy of 42 MeV. This includes the BPMs in FFA loop as well as the BPMs between the main linac cryomodule (MLC) and the dump line.

Turn	Energy (MeV) a=accelerating d=decelerating	Delay from first turn (number of 1300 MHz RF periods, 0.76923 ns/period)	Delay from first turn (number of 398.387 MHz ADC periods, 2.51012 ns/period)
1	42 (a)	0	0
2	78 (a)	343	105.1129
3	114 (a)	686	210.2258
4	150 (a)	1029	315.3387
5	114 (d)	1372+2.5=1374.5	421.2177
6	78 (d)	1715+2.5=1717.5	526.3306
7	42 (d)	2058+2.5=2060.5	631.4435
8 (BPMs between MLC and dump line only)	6 (d)	2401+2.5=2403.5	736.5565

Table 2. BPM timing delays referenced from the first energy pass.

The BPMs that are part of the loop between the injector cryomodule (ICM) and the MLC see a first pass energy of 6 MeV. So for those BPMs the turn 1 energy is 6 MeV accelerating and the turn 8 energy is 42 MeV decelerating. However, the delay times in the table for each turn number are correct for those BPMs as well.

Turn 8 does not pass any of the BPMs in the FFA loop, so as shown above, turn 8 is relevant to the BPMs between the MLC and the dump line only.

Note that none of the energy passes have the same phase of the 398.387 MHz ADC clock (the fractional portion of the delay time), so the timing phases must therefore be different for each energy pass. Thus only one of the 8 energies can be measured at a time, and timing values must change in order to measure different energies.

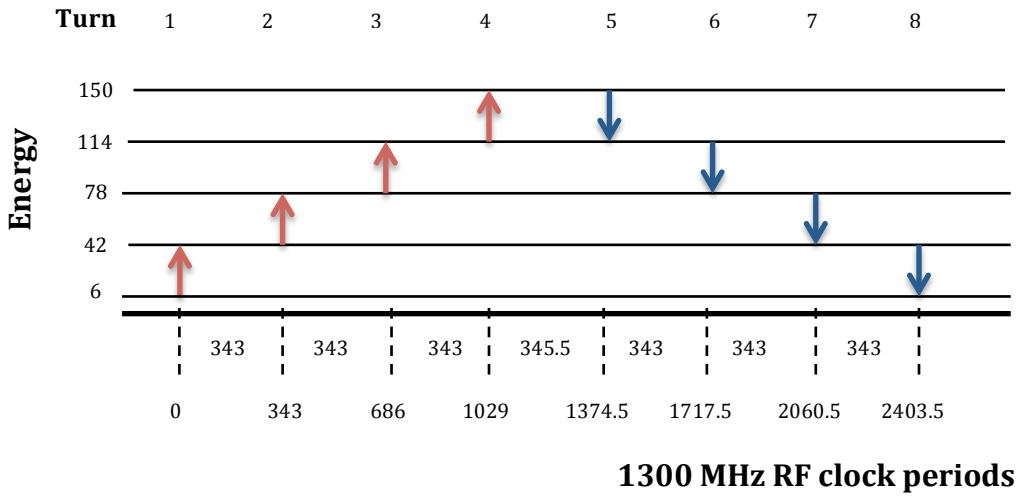


Figure 12. Diagram of pilot bunch spacing between turns as seen at a BPM immediately after the MLC showing all energy passes.

The number of 1300 MHZ RF clock periods between each turn for the first to 4th turn (accelerating) is 343, between the 4th and 5th turn (accelerating to decelerating) is 345.5, and between each turn from the 5th to 8th turn is also 343. The total time from turn 1 to turn 8 is 2403.5 1300 MHz clock periods for a total of 8 different energy passes (figure 12).

For BPMs in the FFA loop, the diagram in figure 12 is identical except the 8th turn (6 MeV) does not exist, so for the FFA BPMs the total time from turn 1 to turn 7 is 2060.5 1300 MHz clock periods for a total of 7 different energy passes (42 MeV, 78 MeV, 114 MeV, 150 MeV, 114 MeV, 78 MeV, and 42 MeV).

Synchronizing data acquisition and delivery between modules

The specific techniques for synchronizing the data acquisition, sequencing of measurements of all the energies, data delivery and time stamping are still under development.

Configuring the timing parameters

The general procedure used to configure the timing for the BPMs is described below. Two levels of profile scanning are required. The first scan level finds the VCO delay timing. However, the peak for each of the 4 channels may be determined to have different VCO delays. Since this is a common parameter, the VCO delay must be the same for all channels, so this first level finds the best VCO delay that works for all 4 input channels. The second scan is performed using a fixed VCO delay, and sweeps though the phase delay range only, thereby finding the phase delay timing for the peak of each input channel.

First level profile scan

1. Click on Full Profile Scan START button - With samples to average set to 5 data will update in about 5 seconds. More average points will take longer.
2. Find the beam peak of interest for timing and set the Peak Find Start Index and End Index to the window of interest.
3. Click Peak Find START to find the timing related to the peak. Results are displayed in the table to the right of the plot.
4. Set the Profile Threshold to a value that is above the noise floor and below the beam signal peak. This is used to prevent writing the timing values for a no-beam condition.
5. Click on Load New VCO Delay. This will write the minimum VCO delay to the hardware. This parameter is common to all 4 channels. The new value will be displayed under VCO Delay.

Second level profile scan

6. Now that the VCO delay is configured correctly, click on START for Fixed VCO delay Profile Scan.
7. Again select the Peak Find Start and End Index for the beam peak of interest.
8. Click Peak Find START to find the Fine Delay Values related to the peak. Results are displayed in the table to the right of the plot.
9. Double check that the profile threshold is correct.
10. Click on Load New Fine Delay. This will write the fine delay values for each of the 4 channels. The newly written values will be shown in the Fine delay row of the table. They should match the Fine delay at peak row. Once this is done, open the V301bpmFAT-plots-raw edm screen. If all is timed correctly, the raw data plots should show amplitudes (in ADC counts) representative of the beam signals.

Button Signal Reflections and Cable Lengths

A reflection of the button signal occurs as the primary signal traverses back from the V301 input to the BPM button and back to the V301 input (figure 13).

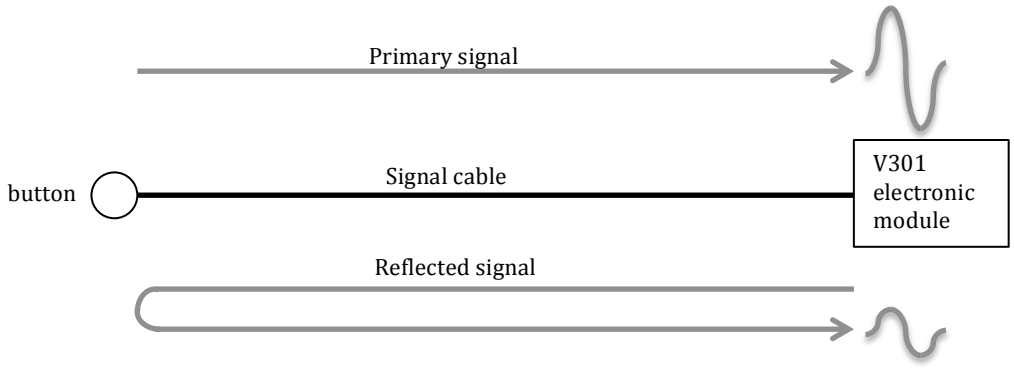


Figure 13. Diagram of BPM button primary signal and reflected signal.

Figure 14 shows a plot of a primary signal and a reflected signal as measured with the V301 electronics. Note that the amplitude of the reflected signal is not insignificant and if it occurs coincident with a bunch being measured, the accuracy of the measurement would certainly be negatively impacted.

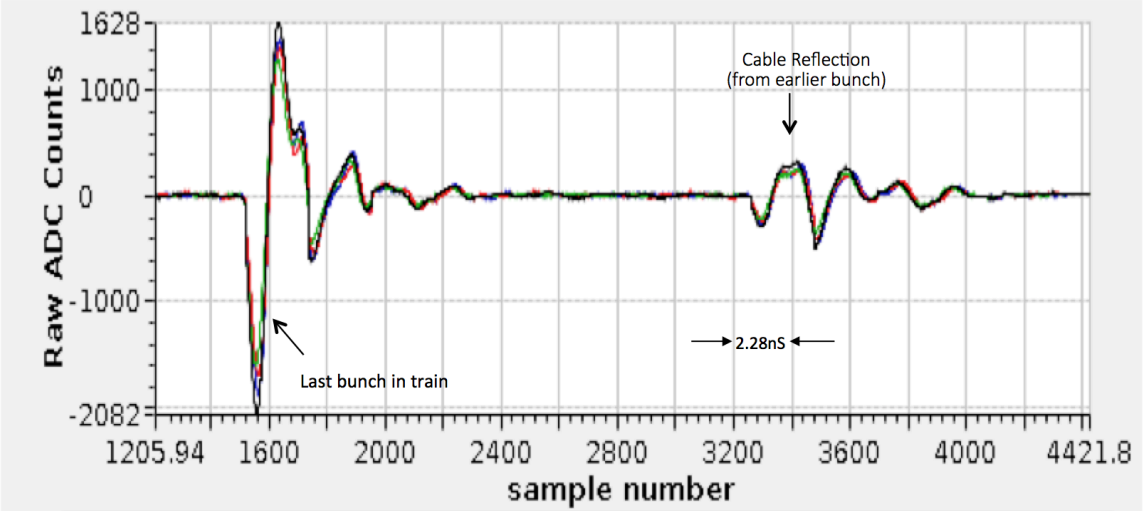


Figure 14. Last bunch of a bunch train followed by a reflected signal from an earlier bunch measured with V301 BPM electronics. The time between samples on the x-axis is about 12 ps.

The BPM cable lengths have been carefully reviewed to understand where the button signal reflections will occur in relation to the BPM pilot bunches being measured.

Figure 15 shows a portion of a typical CBETA fill pattern turn with 6 pyramid bunch trains followed by one pilot bunch train. The two bunches in the pilot bunch train are used for BPM measurements.

Assuming a cable length delay of exactly 5 pyramid bunch trains (1/41.9 MHz * 5 = 119 ns), the bunches shown with red Xs would generate reflections coincident with the pilot bunches used for BPM measurements. Since this is undesirable, the reflections plan to be eliminated by providing a hole in the bunch pattern as shown in figure 16.

Based on this analysis, the cable length for all the BPM signals will be chosen to be 5 pyramid bunch trains.

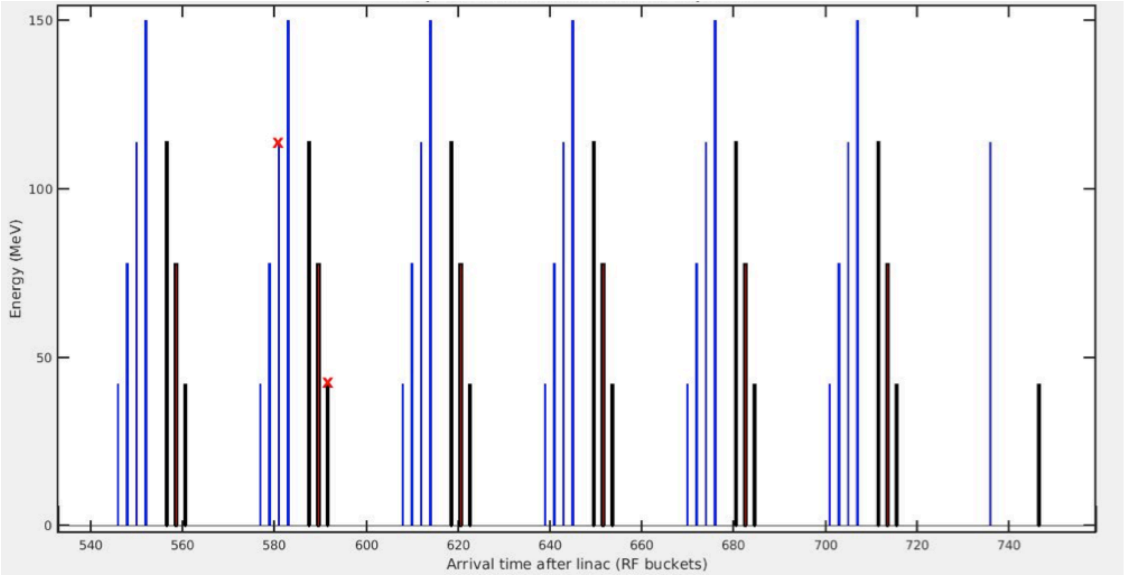


Figure 15. A portion of one turn of the CBETA fill pattern showing 6 pyramid bunch trains (3 accelerating energy bunches shown in blue and 3 decelerating energy bunches shown in black), followed by a pilot bunch train.

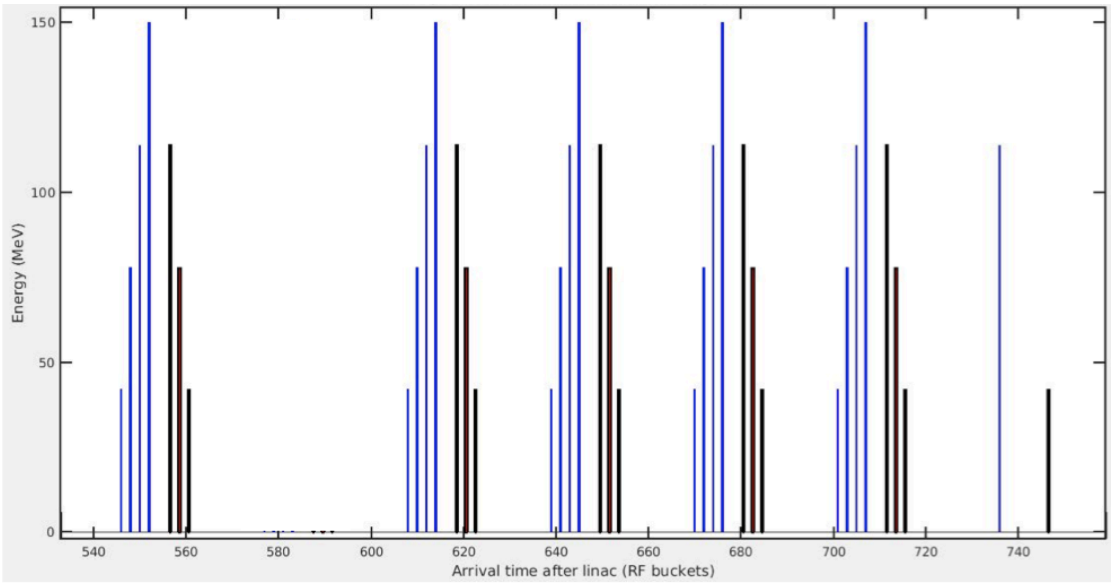


Figure 16. Same image as figure 15 above, but showing a hole in the fill pattern to prevent button reflected signals from affecting the pilot bunches used for BPM measurements.

Fractional arc test images

Several images are provided below showing some of the BPM EDM screens, as well as data plots of BPM data taken during the fractional arc test.

Figure 17. Image of the EDM screen used to configure the BPM timing, showing beam data during fractional arc test (May 19, 2018), with a bunch spacing of 20 ns and ~10pC/bunch. The IS1BPM01 and IS1BPM02 plots are for a fixed VCO delay scan which sweeps the fine delay values only for a total range of about 600 ps. The IS1BPM03, IS1BPM04 and IS1BPM05 plots are for a full profile scan where both the VCO delay values and the fine delay values are swept through the full range of about 2.5 ns.

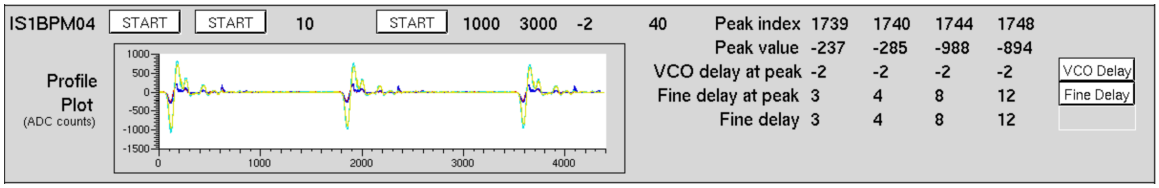


Figure 18. Beam profile scan of IS1BPM04. The optimal timing values for each negative peak are calculated and displayed. These values are written to the hardware by clicking the VCO Delay button to write the VCO delays and by clicking the Fine Delay button to write the fine delay values. For this scan the peak find is calculated using data from ADC sample number 1000 to 3000.

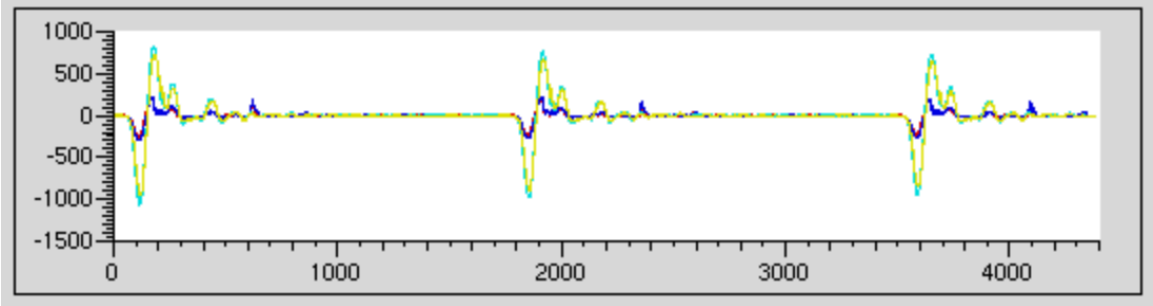


Figure 19. Larger view of IS1BPM04 beam profile scan. The y-axis is ADC raw counts and the x-axis is the sample number, where the time between each sample is ~12 ps.

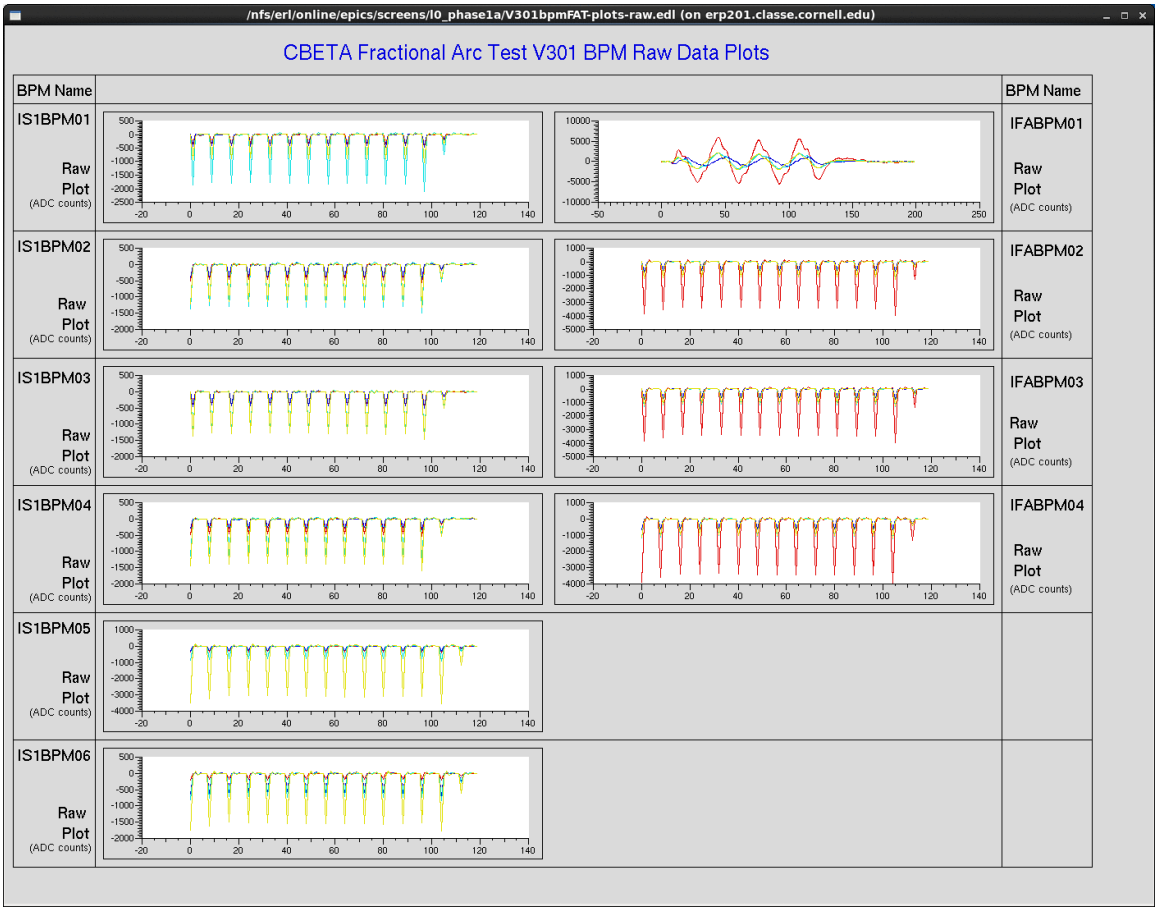


Figure 20. Plots of raw BPM ADC data with timing configured to the peak of each bunch during fractional arc test. Bunch train is about 15 bunches, with 20 ns spacing between bunches. Note the 12.5 MHz waveform for IFABPM01. This module had the BAM filter/mixer chassis connected. Both position and phase measurements are calculated with this 12.5 MHz signal. All other modules calculate position only.

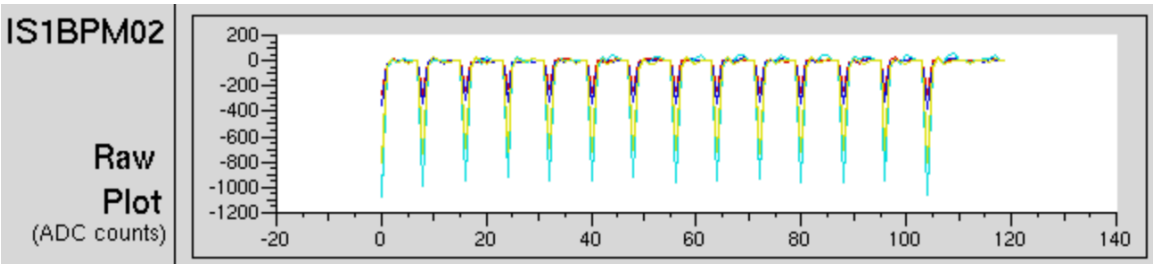


Figure 21. Raw plot of IS1BPM02 ADC data for beam during fractional arc test. Time between samples is one ADC clock, 2.5 ns. The time between bunches was 20 ns (50 MHz bunch rate), so a bunch is detected every 8 ADC samples.

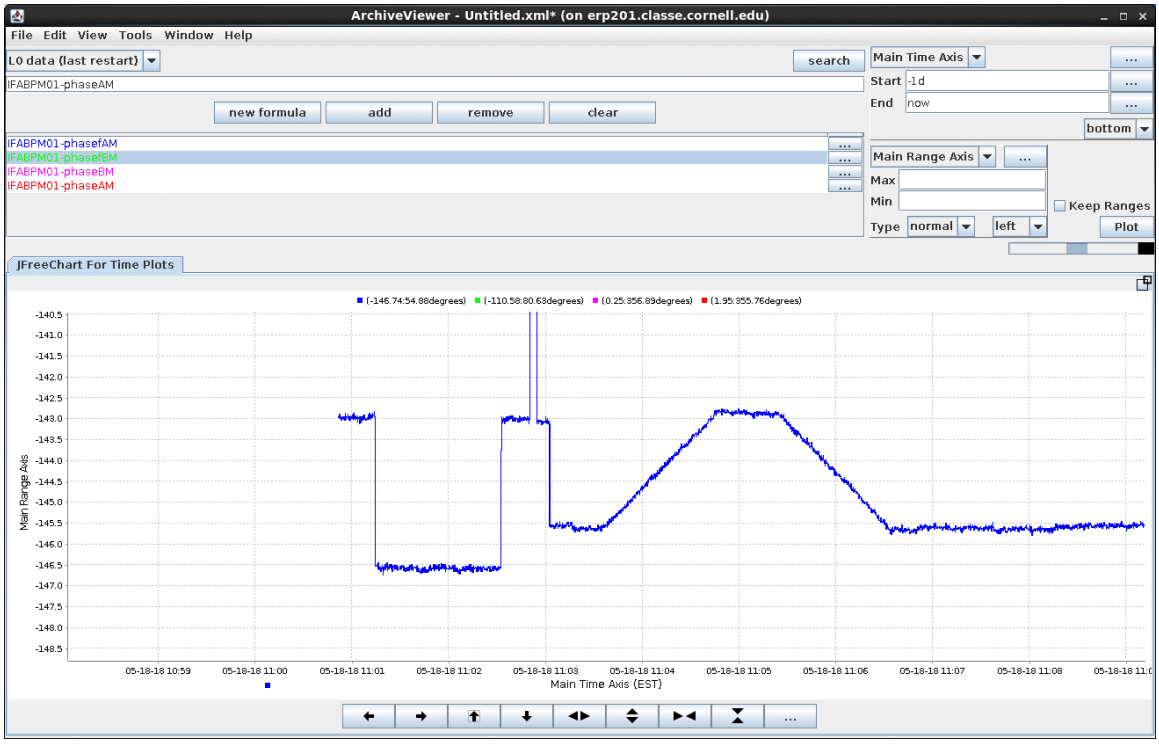
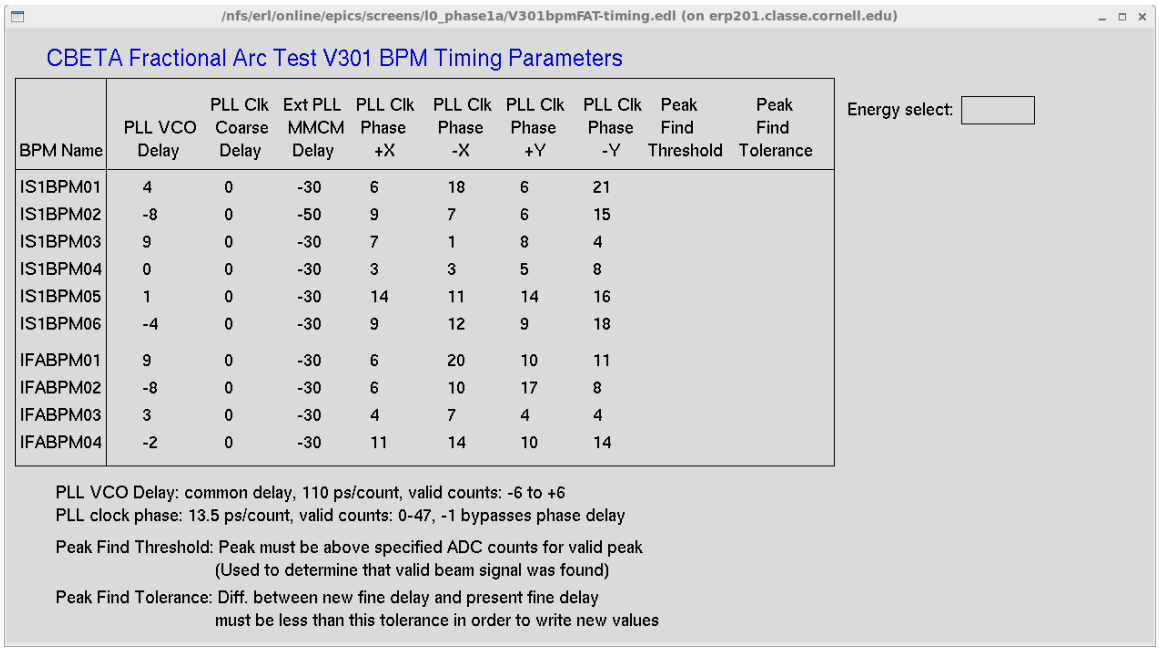
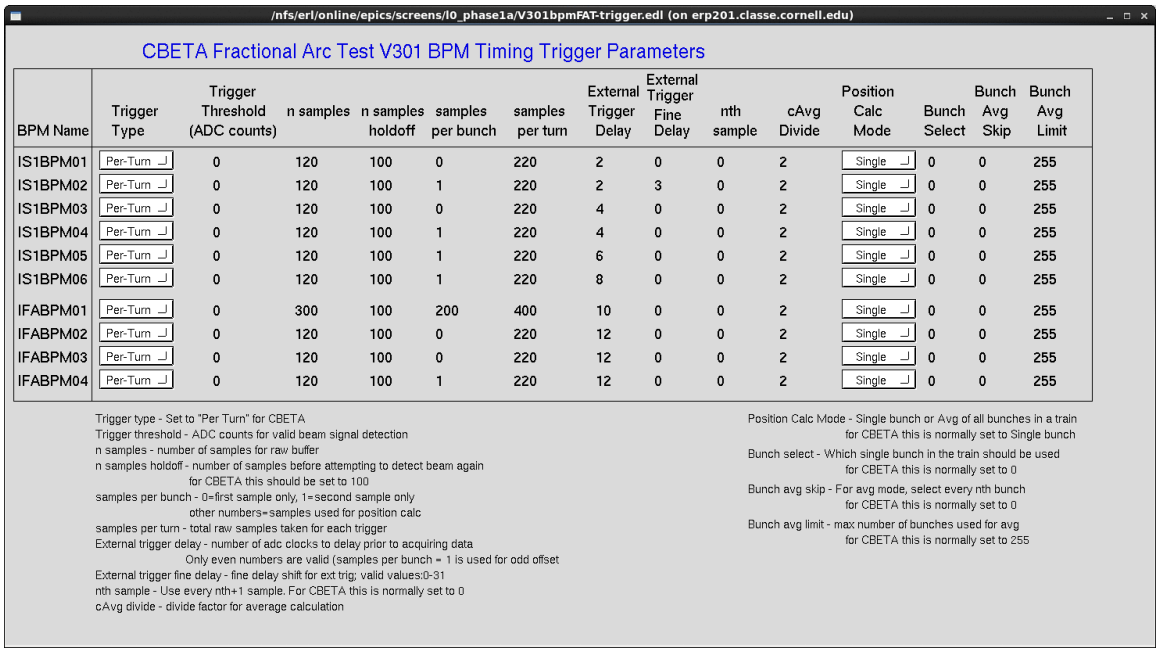


Figure 22. Phase measurement as calculated in the V301 FPGA while machine conditions are varied. These phase variations accurately corresponded with variations of the splitter path length via the motor controlled sliding vacuum joint. The Y-axis is phase in degrees.



BPM Name	PLL VCO Delay	PLL Clk Coarse Delay	Ext PLL MMCM Delay	PLL Clk Phase +X	PLL Clk Phase -X	PLL Clk Phase +Y	PLL Clk Phase -Y	Peak Find Threshold	Peak Find Tolerance
IS1BPM01	4	0	-30	6	18	6	21		
IS1BPM02	-8	0	-50	9	7	6	15		
IS1BPM03	9	0	-30	7	1	8	4		
IS1BPM04	0	0	-30	3	3	5	8		
IS1BPM05	1	0	-30	14	11	14	16		
IS1BPM06	-4	0	-30	9	12	9	18		
IFABPM01	9	0	-30	6	20	10	11		
IFABPM02	-8	0	-30	6	10	17	8		
IFABPM03	3	0	-30	4	7	4	4		
IFABPM04	-2	0	-30	11	14	10	14		

Figure 23. EDM BPM timing configuration screen used for the fractional arc test.



BPM Name	Trigger Type	Trigger Threshold (ADC counts)	n samples	n samples holdoff	samples per bunch	samples per turn	External Trigger Delay	External Trigger Fine Delay	nth sample	cAvg Divide	Position Calc Mode	Bunch Select	Bunch Avg Skip	Bunch Avg Limit
IS1BPM01	Per-Turn	0	120	100	0	220	2	0	0	2	Single	0	0	255
IS1BPM02	Per-Turn	0	120	100	1	220	2	3	0	2	Single	0	0	255
IS1BPM03	Per-Turn	0	120	100	0	220	4	0	0	2	Single	0	0	255
IS1BPM04	Per-Turn	0	120	100	1	220	4	0	0	2	Single	0	0	255
IS1BPM05	Per-Turn	0	120	100	1	220	6	0	0	2	Single	0	0	255
IS1BPM06	Per-Turn	0	120	100	1	220	8	0	0	2	Single	0	0	255
IFABPM01	Per-Turn	0	300	100	200	400	10	0	0	2	Single	0	0	255
IFABPM02	Per-Turn	0	120	100	0	220	12	0	0	2	Single	0	0	255
IFABPM03	Per-Turn	0	120	100	0	220	12	0	0	2	Single	0	0	255
IFABPM04	Per-Turn	0	120	100	1	220	12	0	0	2	Single	0	0	255

Figure 24. EDM BPM trigger timing configuration screen used for the fractional arc test.

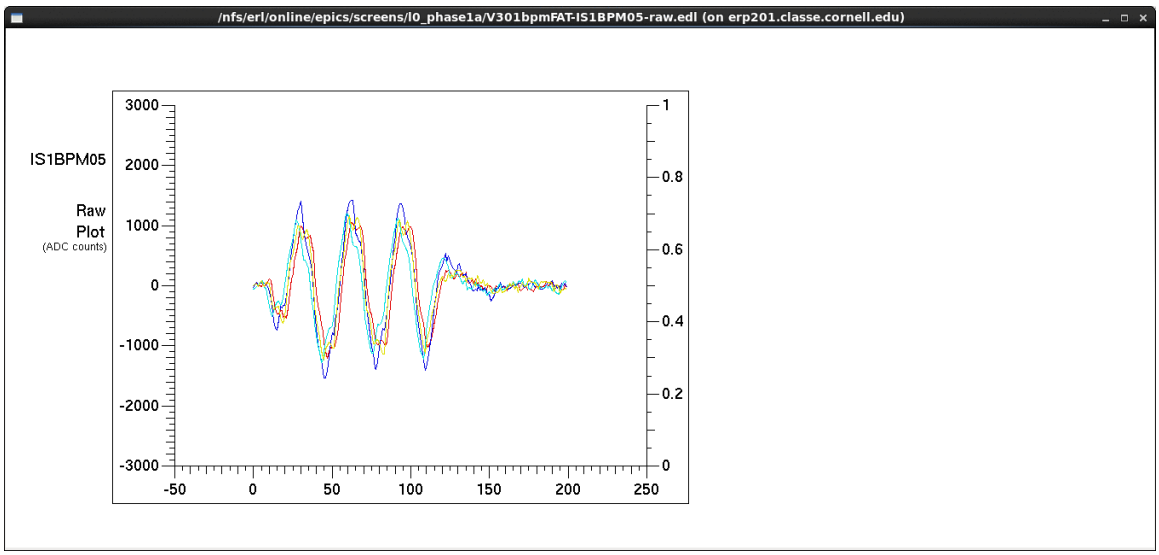


Figure 25. Signal after BAM mixer chassis as measured with V301 electronics. X-axis is ADC sample with 2.5ns between samples. This is with a bunch train of about 15 bunches at 50 MHz (20 ns bunch spacing). Note that the full signal length is about 150 2.5 ns samples or about 375 ns.

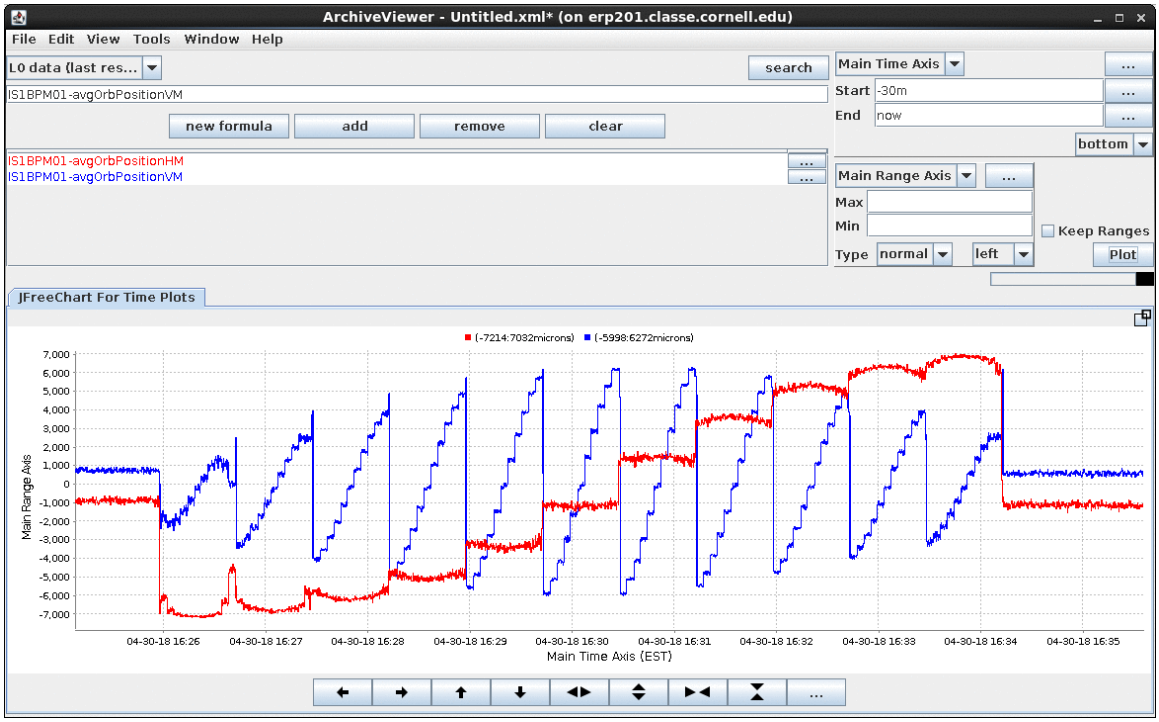
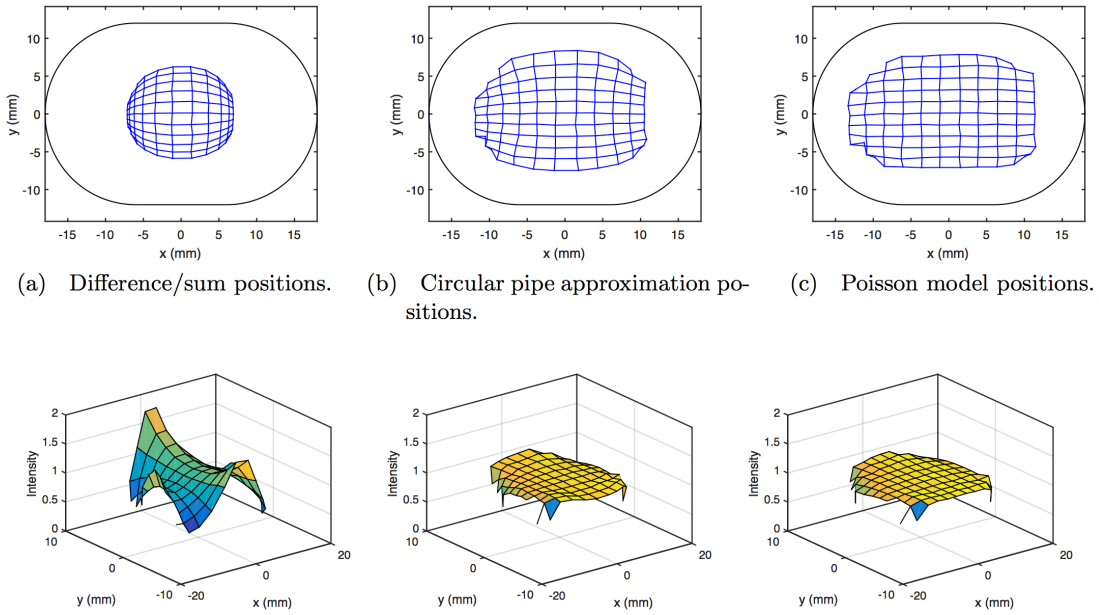


Figure 26. Plot of raw data for IS1BPM01 in splitter 1 while performing a raster scan of beam during fractional arc test on April 30, 2018.

The following image was copied from the CBETA Fractional Arc Test report [3] and shows how the BPM data during the fractional arc test was used to develop and test an acceptable method for converting the raw BPM data to position for the oval BPM button chambers in splitter line 1. The Poisson calculation [4] used in the right most plots will be used for the CBETA position calculation.



(a) Difference/sum positions. (b) Circular pipe approximation positions. (c) Poisson model positions.

(d) Difference/sum intensities. (e) Ccircular pipe approximation intensities. (f) Poisson model intensities.

Figure 3.3.1: Comparison of the beam positions and intensity using three different models to interpret the raw data from the BPM. First, a simple difference/sum model is used. Next, a correction is made using an approximation for a circular pipe. And finally, the model using a fieldmap from a Poisson calculation of the correct 2D pipe geometry is used.

References

[1] R. Hulsart, P. Cerniglia, N.M. Day, R. Michnoff, Z. Sorrell, A versatile BPM signal processing system based on the XILINX ZYNQ SOC, International Beam Instrumentation Conference (IBIC'16), Barcelona, Spain, September 2016

[2] Hoffstaetter, G. H., Trbojevic, D., Mayes, C., Banerjee, N., Barley, J., Bazarov, I., Bartnik, A., Berg, J. S., Brooks, S., Burke, D., Crittenden, J., Cultrera, L., Dobbins, J., Douglas, D., Dunham, B., Eichhorn, R., Full, S., Furuta, F., Franck, C., Gallagher, R., Ge, M., Gulliford, C., Heltsley, B., Jusic, D., Kaplan, R., Kostroun, V., Li, Y., Liepe, M., Liu, C., Lou, W., Mahler, G., Meot, F., Michnoff, R., Minty, M., Patterson, R., Peggs, S., Ptitsyn, V., Quigley, P., Roser, T., Sabol, D., Sagan, D., Sears, J., Shore, C., Smith, E., Smolenski, K., Thieberger, P., Trabocchi, S., Tuozzolo, J., Tsoupas, N., Veshcherevich, V., Widger, D., Wang, G., Willeke, F. and Xu, W. [2017]. CBETA Design Report, Cornell-BNL ERL Test Accelerator, *ArXiv e-prints* .

[3] C. Gulliford, et al., The CBETA Fractional Arc Test, September 2018

[4] A. Bartnik, Nonlinear BPM Positions using Poisson, July 2016