CBN 99-20

LONGITUDINAL FEEDBACK AT CESR*

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Abstract

Total stored electron and positron beam currents at the Cornell Electron Storage Ring (CESR) have been limited by the presence of a dipole multibunch longitudinal instability having a threshold at approximately 250mA of total current. A longitudinal feedback system has been under constant development, test, operation and upgrade over the past several years. The result has been an increase in the High Energy Physics (HEP) operating current to over 500mA total. This paper describes the overall design of the present system, using a horizontal stripline kicker to produce combined horizontal and longitudinal bunch by bunch beam stabilization. Some details on specific subsystems, including: receiver design, individual bunch phase DC offset correction, digital signal filtering, and the RF modulator will be given, as well as an outline of plans for further development.

1 INTRODUCTION

The CESR Storage Ring has been colliding short trains of electrons and positrons since 1995. Each beam consists of 9 trains of up to 5 bunches, with a minimum bunch spacing of 14ns. The spacing between bunch trains is either 280 or 294ns in a quasi-uniform pattern over the 2.56µs revolution period. The positron and electron beams circulate in the same beampipe, separated by pretzeled orbits, and collide in a single interaction region.

In April 1996, during HEP operation with nine trains of two bunches, a longitudinal instability appeared when total currents were above 250mA. Although the instability threshold current depended somewhat upon bunch spacing[1], RF cavity parameters, orbit and other variables, active feedback was required in order to make significant increases above 250mA total.

2 SYSTEM OVERVIEW

A block diagram of the present longitudinal feedback system is given in Fig. 1. A Beam Position Monitor (BPM) signal is filtered and phase detected using the same 500MHz reference that is used by the CESR RF system. The result is amplified and sent to a Digital Signal Processor (DSP) which samples and filters the data from each bunch. The DSP output is converted back to an analog signal that is further processed and amplified. In the present system, a horizontal kick at a point of dispersion is used to produce a longitudinal impulse [2]. The error signals from the longitudinal and horizontal feedback systems are combined to yield a single horizontal output kick for each bunch.

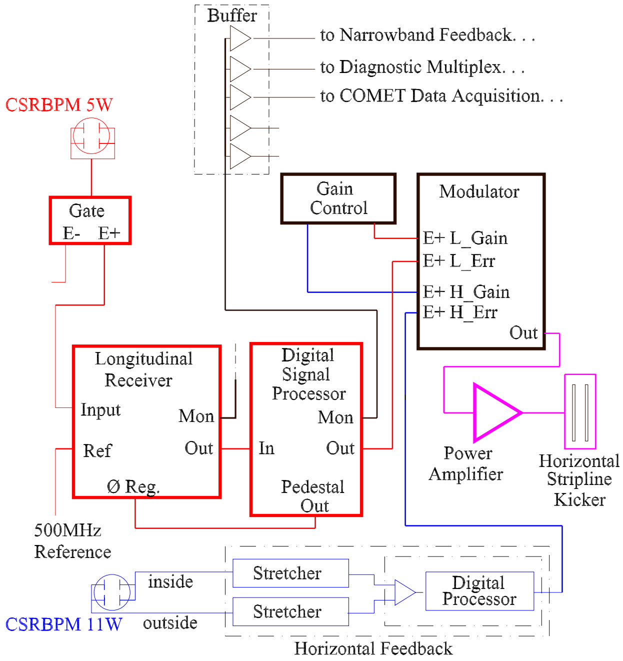

Figure 1: Block diagram of the combined horizontal and longitudinal feedback systems (positron channel shown).

3 SYSTEM DESIGN

Given the maximum output voltage provided by an amplifier, the maximum loop gain of the system will be limited by signal to noise ratio, beam transients, or DC offsets. The signal to noise ratio fixes the gain at which receiver noise begins to saturate the output amplifier. Further increasing the low-level gain only increases the proportion of the noise-saturated signal, resulting in little or no increase in system gain. The presence of beam transients (primarily of the zero mode) can produce an error signal exceeding the system's dynamic range and make the system insensitive to small higher frequency mode oscillations. DC phase offsets, e.g. due to beam loading with unequal bunch currents, will saturate the system unless they are properly nulled. The following subsections describe the feedback system in more detail, and outline how system gain was maximized.

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3.1 *Pickup, Filters and Gating*

The signals from four capacitive buttons are combined in order to minimize the sensitivity of the detector to transverse motion, which can be much larger than the longitudinal transient produced during injection. The button signals are first combined in pairs using 100Ω striplines to a 50Ω tee. The signals from the two tees are then combined in a terminated tee and the result sent to the feedback electronics using heliax cable. At typical operating currents in the region of 5 to 10mA per bunch (.5 to 1.0×10^{11} Particles), the beam signal at the input to the feedback electronics is a bipolar pulse with a peak voltage of roughly 16V. After filtering, using a lowpass 0.6ns quasi-gaussian filter[1], the signal is about 5V peak.

Since both beams are counter-rotating in a single pipe, the positron and electron bunch signals are present in the same cable. The positron and electron signals are demultiplexed using a GaAs switch to allow processing by separate hardware. The maximum filtered signal level that can be handled by the GaAs switch is roughly +20dBm (1dB compression point), which requires that the button signal be attenuated by 16dB.

In addition to minimizing sensitivity to transverse motion, the signal combination scheme gives a minimum of reflections over a very wide bandwidth. This is crucial, since reflections will appear at an arbitrary phase. After phase detection, signal amplifiers could saturate on these unwanted variations rather than on the error signal itself.

3.2 *Longitudinal Receiver*

In the longitudinal receiver the phase of the bunch signal is mixed with a 500MHz reference signal (the same reference used by the CESR RF cavities). The reference signal is routed through a voltage controlled phase shifter controlled by the sum of an offset voltage, a regulation voltage, and an external modulation signal. The offset voltage can be adjusted via the control system computer to bring the phase shifter control voltage into regulation.

The phase regulation error signal comes from the DSP pedestal output (see section 3.3), which is the sampled phase offset of each bunch. The phase regulation loop has a bandwidth of <10 kHz , so it regulates on the average of the pedestal signal from all of the bunches, and therefore on the average bunch phase. The phase error signal is low pass filtered, amplified, and sent to the input of the DSP.

The maximum signal voltage that can appear at the input to the mixer without causing receiver distortion is +23dBm, roughly coinciding with the maximum signal handling capability of the GaAs switch in the previous gating stage. The sensitivity of the present receiver is about 280mrad/volt, with a maximum output of +/- 1Vpp. The noise output of the receiver is about 10mV (sigma) at 5mA/bunch or about 2.8mrad. However, the measured phase noise of the 500MHz reference is much larger than this, 12mrad[3]. Presumably, 1/f noise from the reference is being filtered by the receiver's phase regulation loop.

3.3 *Digital Signal Processor*

The digital signal processors reside in a VME crate, one VME board for the electrons and another for positrons. An analog gain of 15 is applied to longitudinal receiver output before being digitized by a 10 bit ADC at 71.4MHz (the maximum practical bunch frequency used in CESR). There are two separate paths for the digitized data: the pedestal correction circuit and the digital filter.

The pedestal correction circuit integrates phase error data from each bunch with a time constant of 8 turns, and passes this data to a DAC and the input opamp, subtracting the result from the incoming signal bunch by bunch. In this way the average signal seen by the ADC will regulate around zero for each bunch. DC phase errors due to the beamloading of uneven bunch currents (e.g. during injection) can easily approach 20mrad. At our present gain settings, the ADC will saturate at about 9mrad, while system gain saturates at 1mrad (amplifier limit). Nulling the DC bunch phase errors increases the gain that can be applied before the error signal is digitized.

The digital filter is constructed of two FIFO memories and two programmable logic devices (PLDs). It contains 183 bandpass and lowpass filters (for 183 bunches/turn). Filter frequencies can be adjusted with a resolution of 0.1kHz near the 20kHz synchrotron sidebands, and the bandpass filter Qs can be adjusted from 3 to about 200 (6 is used in operation). Registers allow the control of the filter parameters via the control system computer and the VME crate microprocessor. Digital filtering reduces the noise on individual bunch signals by about 20dB, allowing a corresponding increase in loop gain. Analog and digital versions of the output signal are available.

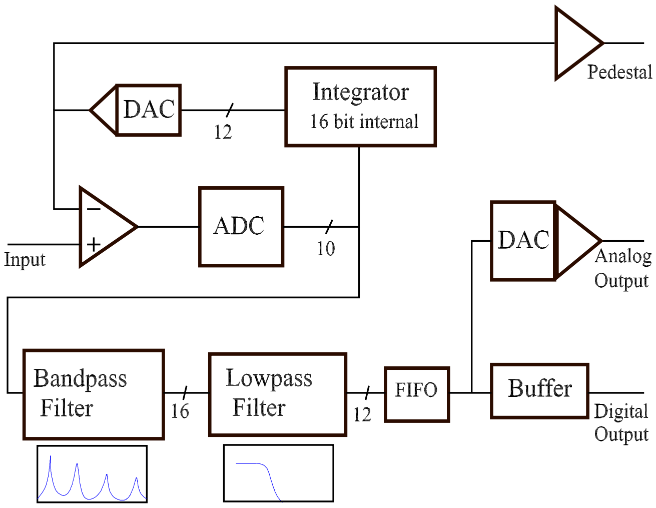

Figure 2: Block Diagram of DSP showing the signal path of each bunch. The output can be delayed up to 16 turns.

[1] Picosecond Pulse Labs. Box 44, Boulder, CO 80306.

3.4 Analog Modulator and Amplifiers

The analog error signals from four feedback channels: e+ and e-, horizontal and longitudinal, are scaled and summed to form a combined horizontal-longitudinal correction kick. Electron and positron signals are time multiplexed. A GaAs switch under the control of the CESR timing system alternately selects positive and negative versions of this combined error signal. This produces a 14ns long bipolar pulse whose amplitude is proportional to the error signal. A limiting signal amplifier ensures that the power amplifier will not be saturated.

The delta output of a 180° hybrid splitter converts a single amplifier output into differential signals that are then applied to the inside and outside plates of a shorted stripline kicker. An advantage of this scheme is a considerable cancellation of beam induced voltages seen by the amplifier [4].

4 SYSTEM PERFORMANCE AND FUTURE PLANS

Amplifier power limited the maximum output voltage to 200V peak. Applied to the horizontal stripline, this results (through dispersion) in a longitudinal output kick of 140V/turn. Given this amplifier output, damping rates of 200sec^{-1} were obtained without digital filtering. Gain could not be increased further since the 1σ receiver noise voltage was at the level corresponding to maximum amplifier output. Once digital filtering of each bunch signal was applied, the reduced noise allowed gain to be increased tenfold, with damping rates now measured at about 2000sec^{-1} ($14\text{sec}^{-1}\text{mA}^{-1}$). This increase in gain gives a corresponding decrease in the linear dynamic range of the system, but we have not yet observed this to be a limitation on the amount of current that can be stored. HEP total currents are now in excess of 500mA total. Table 1. compares the phase error that produces system saturation (on amplifier maximum voltage) with the errors observed in operation. This points out the necessity of nulling the DC phase offsets.

Measurements indicate that the dominant longitudinal excitation during injection is of the zero mode, at a level that is well beyond system saturation at the peak of the transient (see Fig. 4). Since the zero-mode is Robinson stabilized, we may filter this lowest sideband from the error spectrum, so that it will not interfere with the damping of other modes.

Further improvements in performance are being explored. The wire-wrapped prototype DSP boards, are being replaced with printed circuit boards with some additional diagnostic features and a zero mode filter. A digital amplifier, with a peak output voltage of 1kV is under test [5], and an RF cavity kicker is being developed similar to that at DAΦNE.

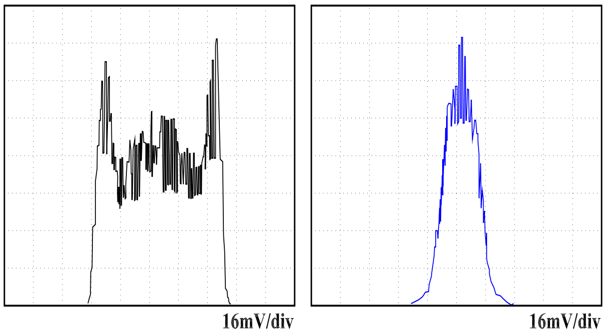

Figure 3: Voltage Histograms of the modulator output showing limiting on receiver noise (left), and the noise reduction after being filtered by the DSP (right). System gain is also four times higher with the DSP installed.

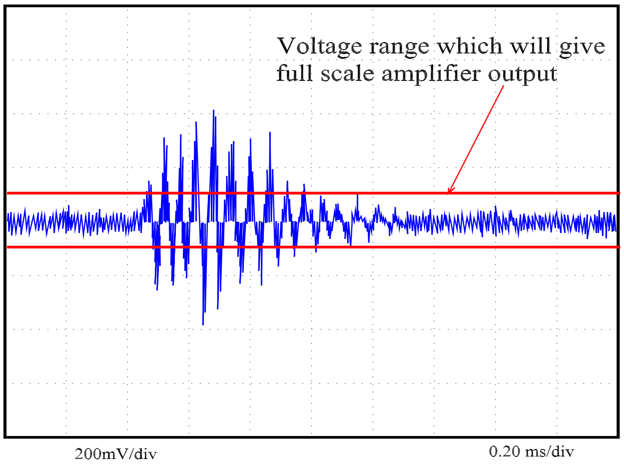

Figure 4: DSP output monitor during an injection transient. System saturation occurs at 100mV or less.

Table 1: Phase errors in the CESR feedback system

Conditions	Phase at 500MHz
System saturation (output amplifier)	1.0 mrad
Receiver output noise sigma	2.8
DSP filtered output noise sigma	0.2
ADC saturation	9.0
Injection transient peak	3.0
DC phases between bunches (max)	20.0

5 REFERENCES

[1] M.G. Billing, *et al*, Observations of a Longitudinal Coupled Bunch Instability in CESR, these proceedings.

[2] D. Sagan, M. Billing, Cornell LNS note CBN 96-06 (1996).

[3] K. Ormond, *et al*, Cornell LNS note CON 96-16 (1996).

[4] J.T. Rogers, *et al*, Proc. 1995 Particle Accelerator Conf.

[5] G. Codner, et al, CESR Feedback System Using a Constant Amplitude Pulser, Proceedings of the 8th Beam Instrumentation Workshop, pp. 552-59.