There will be detector tour Tuesday, November 9 at 9:30. Meet in the DAQ Lab just before 9:30, and we will go down and look at the DR readout hardware.

Things to Remember

- Always be sure power is off to a crate before inserting or removing cards. FASTBUS claims to be “hot-swappable” – we choose not to test this feature.
- It is safe to plug in or remove cables from the front-panel of cards while they are powered.
- Be careful not to short pins together when using a scope probe to look at pins of an IC.
- Prevent the ground lead on the scope probe from touching parts of the board. Securely connect it to “board ground” (not necessarily chassis ground).

Monday: Getting to Know the Test Stand

Goals: recognize the various components of the test stand and how they are representative of components in the real online system, run a few “high-level” diagnostic packages to become familiar with computer interface to readout and slow control

- Identify the TQT, Fastbus, and VME crates. Examine cable routing – look at signal path from preamp to TQT to TM to TDC. Look also for SBUS and Timing System controllers and modules. What is the link between the Fastbus and the VME crate? How does this compare to what is used in the real system?
- What is the address of the TQT crate? Make note of the slot numbers for the TQT and TDC board.
- Power up the test stand and connect an axial preamp to the TQT input.
- Logon to `vnet58` (the CPU running in the VME crate). Type `moduleShow` to see the currently loaded modules. The table should be empty. To load the code needed for our test stand diagnostics run the script `~mrs43/daq/scripts/loadAll` by typing `~mrs43/daq/scripts/loadAll`. Type `moduleShow` again and look at what modules you have loaded. VxWorks will allow you to execute any function in the modules you have just loaded directly from the command line. Start the main loop of the `checkPreamp` program by typing `checkPreamp`.
- Type `vdb` to read the ADC on the TQT board. What is the power-up value for the preamp voltage? By using the schematic for the front panel connector on the TQT board or the preamp use a multimeter to verify the preamp power.
• Axial preamps typically are set to run around 3.4V while stereo run at 3.0V. Use the command \texttt{vpre} to reset the preamp power for this preamp to 3.4V. On the TQT board the preamp voltage is set by an 8-bit DAC. The number that you pass to \texttt{vpre} is therefore a DAC setting between 0 and 255. Explore range of available preamp voltages using this DAC. Use the multimeter to watch voltage changes. What DAC setting generates a preamp power setting of roughly 3.4V?

• Use the command \texttt{qped} to measure and record the charge pedestals for the channels. Try moving the preamp around or touching parts of it while doing the measurement. Does the amount of noise change?

• Use the command \texttt{qlin} to measure and record the linearity of the channels. The slope reported is in units of TDC counts per volt of calibration pulse.

• Now use the command \texttt{pulse} to pulse the channels. This command delivers a calibration pulse to all channels and reads out the time and charge hits. Use the measured charge hit along with the pedestals and slopes recorded above to compute the calibration pulse voltage. How does the spread of the computed calibration pulse voltage compare with the spread of the absolute charge hit across the 12 preamp channels?

• Disconnect the preamp from the TQT board and hook up the LeCroy pulser. Understand the components of the pulsing circuit. From which timing signal is the pulser trigger derived? You can figure this out by looking at the TQT controller schematic. Note that the CPU can talk to the pulser through a GPIB (General Purpose Interface Bus) card in the VME crate.

• Quit \texttt{checkPreamp}, and start \texttt{checkTQT}.

• Measure charge pedestals using \texttt{qped}. Are the pedestals for the 12 channels you measured above still the same value?

• Measure the linearity of the channels using \texttt{qlin}. The reference board you are using is the only board that has not had the charge gain modification made to it. While the linearity check is in progress you can watch the pulse size on the pulser ramp up. The results of the linearity check will be written to /home/tom/daq/data/TQT/raud/charge.dat. The format is:

\begin{verbatim}
<pulser level> <avg. ch. 0> <rms ch. 0> ... <avg. ch. 47> <rms ch. 47>
\end{verbatim}

Using a separate shell copy this file somewhere to your home directory for safe keeping.

• Remove one of the attenuators on the pulser output and rerun the linearity check. This will now saturate the charge measurement circuit. Again, copy the resulting \texttt{charge.dat} file to your area.

• You can now turn off the test stand.

• Using the two files and Excel, PAW, ROOT, or some other package:
  
  – Plot charge hit vs. pulser voltage for several channels in both of the files. Do you see what you would expect? Where to charge circuits begin to saturate?
  
  – In the file where you do not saturate the charge integration circuit do a linear fit to each channel. The y-intercept of this fit is effectively the pedestal. What is the variation in pedestal across the board? Is it random or systematic? Can you explain what you see?
Tuesday: Understanding the TQT

- Setup the test stand with the TQT board on the extender card. Turn on the test stand and start up `checkTQT`.
- Use `checkTQT` to measure and record the width of the timing pulse.
- Use the command `tsloop` to put the system into a continuously looping mode. This will allow you to look at the analog signals on the board.
- Find and measure the width of the timing pulse with the oscilloscope. Does it agree with what you measured using the TDC?
- Find and observe each of the signals on the timing diagram below:

![Timing diagram](image)

- Using the oscilloscope measure saturation point of the charge circuit with respect to pedestal and also the slope of the charge circuit. Do the measurements agree with what you measured from the output of `qlin` yesterday?
- A quick logic analyzer exercise: We discussed the 32-bit SBUS address cycle during the TQT lecture. The first 16 bits are crate and card, while the last 16 bits are a code for the component you would like to address. In the example in the lecture, the code to write to the ADC was 0x0101. Use the logic analyzer to determine the code to reset the DACs on the TQT board. (You can reset all of the DACs on the TQT board from the VxWorks command line by typing `dac8801reset( 62, 8 )`.)
Wednesday: Understanding the TDC

- Remove the extender card and put the TQT board into slot 8 of the TQT crate. Insert an additional TDC into one of the higher slots of the crate.
- Startup checkTQT and run the qlin command. This will put the timing system in a mode so that we can pulse the TQT board using the LeCroy pulser.
- Patch one channel from the TQT→TDC cable into the TDC that you loaded.
- Quit checkTQT and startup checkTDC. Use the command fpcom and the scope to verify that when you send a front panel common stop signal, a trigger pulse is sent to the LeCroy pulser.
- Reset the board using reset and use csr to verify the startup values of the control-status registers.
- By writing to the status registers configure the TDC to register rising and falling edges of pulses, run in common stop mode, and enable the front panel common input.
- Use fpcom to generate an event with the timing system. Verify that the write pointer to the page in the circular buffer has been incremented.
- Use lne (Load Next Event) to load the event you just generated. Verify that the read pointer has incremented.
- Use read (not readout) to read the event. Is the timing hit spacing what you measured on the scope yesterday?
- Measure the slope of the charge circuit by dialing up the pulser and using fpcom to generate events. Fill the circular buffer with 8 events. Then readout the 8 events by using readout (readout combines the lne and read commands). Is the slope roughly what you saw yesterday?
- Estimate pedestal for the channel you are studying and write a suitable sparsification value for this channel, to do this:
  - disable commons in CSR0
  - disable sparsification in CSR1
  - write the value to CSR 0xC00000XY where XY goes from 00 to 5F and specifies which channel you want to sparsify (you’ll have to convert this to an integer for the WCSR command!)
  - re-enable commons and “simple” sparsification (bit 9) CSR0
  - re-enable sparsification in CSR1
- Set the TDC to register just rising edges. By varying the pulse height on the pulser verify that when no charge is injected no hits are registered on the TDC and when charge is injected two hits are registered in the TDC.
- Lengthen the cable from the timing card to the fanout board in the TDC crate. What is the corresponding shift in the location of the timing hit? Can you measure the speed of light in the cable?