Proposal to the University Consortium for a Linear Collider

August 30, 2002

Proposal Name

Development and design of an LC ASIC for CCD readout and data reduction

Classification (accelerator/detector: subsystem)

Vertex Detector

Personnel and Institution(s) requesting funding

Boston University, Physics Department: Ulrich Heintz (asst. professor)

University of Oklahoma at Norman, Department of Physics: Patrick Skubic (professor), Rusty Boyd (engineer)

Collaborators

William Wester, Fermilab

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Project Overview

A high-resolution vertex detector is a crucial component of the detector for a future linear collider. An impact parameter resolution $\sigma \approx 5\mu\text{m} \oplus 10\mu\text{m GeV}/p \sin^{3/2}\theta$ is desired both in $r-\phi$ and z for flavour tagging that identifies tracks coming from primary, secondary or tertiary vertices created by the decay of particles in an event [1]. Charge coupled devices (CCD) are the most established technology for large-scale pixel vertex detectors. The SLD experiment has succesfully operated a 307 Mpixel CCD vertex detector [2]. The major challenges for a CCD based vertex detector at a future linear collider are in three areas:

- reducing the amount of material by thinning the substrate;
- improving radiation hardness;
- increasing the readout speed.

This proposal will address the third challenge - readout speed. We propose to develop a readout system that will demonstrate the feasibility of use of CCD's at the LC, and could lead to designs for specific experiments. Other technologies that potentially have resolutions competitive with CCD's may also be investigated. We will collaborate with groups in the US and Europe that are developing CCD detectors for the LC. We will readout the CCD's being studied the the Oregon/Yale group, and those under development for Tesla by the Linear Collider Flavor Identification (LCFI) Collaboration in Europe. Some discussion with both groups has been started.

For the vertex detector of the SLD experiment, VXD3, there were 307 million CCD pixels[2]. The electronic circuitry that was used to handle this large number of pixels was complicated, involving at least 8 to 10 FPGA chips that were on FASTBUS modules. Readout of the SLD vertex detector took about 200 ms. For a linear collider application this time must be reduced by three orders of magnitude. To be able to read out the LC vertex detector it will be necessary to suppress pedestals on detector and replace some (or all) of the FASTBUS module functionality with much smaller and faster circuits, possibly contained in a single chip. A parallel readout architecture will have to be implemented.

We propose an R&D program that starts with the detailed study of the present VXD3 design developed at SLAC, and other pixel detectors to understand them thoroughly and will work in collaboration with Fermilab to develop ASIC's with improved performance. The proposed work would lead to the design of a highly efficient system, which can be used to improve the electronic performance and hence the accuracy of the detector. In order to test our chips, we propose developing a DAQ test station suitable for detector and readout bench/beam tests.

This effort builds upon previous VLSI work at University of Oklahoma. Five EE Masters students completed theses on VLSI related projects as members of our group. This includes the complete design, fabrication and testing at OU of 4 generations of a mixed-mode analog multiplexer IC, the VAMUX, which was used in the CLEO III, silicon sensor QA system. Three students contributed to the development of the ATLAS pixel detector front-end readout chip, in collaboration with LBNL. We have educational licenses for Cadence and other design tools.

We have had considerable experience with Maxwell Spicelink, which is a software package which can be used extract the L, C and R parameters of metal traces and their electromagnetic interactions with surrounding materials, such as Si and dielectrics. Maxwell creates a Spice model of the circuitry from a 3-D drawing by solving the field equations using finite element analysis. This spice model can then be used in circuit simulations. These simulations would be very useful in evaluating designs of CCD's that can be read out at very high speeds, such as proposed for Tesla.

Boston University has previous experience with irradiation tests, design, and construction of the silicon strip detector for DØ and high-speed digital electronics for the level 2 silicon track trigger for DØ. We will draw on the Electronics Design Facility at Boston University [5] as a resource, which has extensive experience in FPGA design (DØ, CMS) and ASIC design (ATLAS). The facility also provides access to the advanced design tools required, such as Mentor and Cadence.

FY2003 Project Activities and Deliverables

Presently, the VXD3 layout consists of three barrels with a total of 96 CCDs on 48 ladders with 4 outputs per CCD yielding a total of 384 outputs. These analogue outputs are digitized and applied with a clocking signal and a bias supply at the front-end (F/E) electronics whereas the FASTBUS modules are used for managing data acquisition and providing timing and control functions. The FASTBUS data acquisition modules are placed at a distance of 50 m from the F/E boards and are connected by optical fibers. For the SLD vertex detector, disruptions in the data link occurred during accelerator operation. For reduction in the amount of devices used and to make the circuit smaller for subsequent improvement in the data processing speed and reliability, we would like to develop a new design. Replacing FASTBUS module functionality with with smaller chips will enable us to place them on the barrel itself, close to the F/E hybrids. This will also make it inaccessible after detector installation, so it has to be completely reliable and able to withstand the radiation environment.

The objective for the first year would be to develop a set of specifications for the ASIC such as modularity, number of gates required for the entire operation and the identification of the design methods and development tools that are appropriate for this project. We will study the use of ASIC's and FPGA's to optimize the design for the LC. The specifications will be developed in close coordination with the Oregon/Yale and LCFI groups working on CCD detector development. We also anticipate fabrication of a small number of test structures through MOSIS in the first year. This would mainly be done by Oklahoma and Fermilab.

In order to test prototype vertex detector elements and/or readout chips a simple data acquisition system is required, that can be operated with minimal infrastructure requirements. The Fermilab Computing Division ESE Group has developed a general purpose set of PCI Test Adapter Cards for the BTeV experiment [3,4] that will form the basis of the BTeV pixel detector test stands. These cards are also used to test the SVX4 readout chip for the silicon strip detectors for CDF and DØ. These cards feature large FPGAs that can be programmed to interact with the device to be tested. It seems that these boards could be very useful for linear collider vertex detector test stands as well. This would mainly be done by the Boston group.

We propose to obtain a few sets of these boards and assemble a test DAQ system, using a PC provided by Boston University. We will understand the capability of the system and learn how to program it. By the end of the first year we intend to have the system running in a sample data acquisition application. This may require the design of an additional interface card for the specific detector. This project is well suited in scope for a graduate student.

FY2004 Project Activities and Deliverables

During the second year the engineers at all three institutions will collaborate in the development of a prototype readout chip for CCDs, following the specifications that were developed in the first year. We intend to use the DAQ system developed in the first year to test these prototype devices.

FY2005 Project Activities and Deliverables

During the third year the design of the readout chip will be finalized using the experience gained from the prototype tests during the previous year. The ultimate goal is to obtain a functional design for a readout chip that establishes the technical feasibility and can serve as the starting point for a production design.

references:

1 J.Brau et al., “Linear Collider R&D” (http://blueox.uoregon.edu/ jimbrau/LC/LCrandd.ps).

2 K. Abe, et al., ”Design and Performance of the SLD vertex detector: a 307 Mpixel tracking system”, Nucl. Instru. and Meth. A400 (1997) 287-343.

3 K. Treptow, G. Deuerling, “PCI Test Adapter Card” (http://www-ese.fnal.gov/eseproj/BteV/TestStands/PCI_Test_Adapter.doc).

4 J. Andresen et al., “Programmable Mezzanine Card (PMC)” (http://www-ese.fnal.gov/eseproj/BTeV/TestStands/PMC/Prgm_MezzanineCard.pdf).

5 see web page at http://ohm.bu.edu/edf.html.

Budget justification

Boston University: We ask for support for a graduate student, who will work 90% on this project during the first year. During the second and third year the student will be 50% on DØ, doing his thesis research and 50% on this project, which will provide the hardware experience that is a crucial part of graduate education in particle physics. The graduate student is charged at the rate for graduate assistentships set by the BU College of Arts and Sciences for FY 2002 ($1812.5/month), increased by an estimated 5% per year thereafter. We are also asking for support for 20% of an electrical engineer starting in the second year at the current subsidized EDF rate of $35/hour (in the other direct costs category). We request travel support for about two trips each in years 1 and 2, and four trips in year 3 to Fermilab or other collaborating institutions for meetings. Indirect costs are calculated at BU's rate of 63%. The equipment budget includes one set of PCI Test Adapter boards ($2000/set) and funds for an interface card ($2500) in the first year and $2500 in the second and third years for fabrication of readout chip prototypes.

University of Oklahoma: We request a modest amount of support to fund an Electrical Engineering Graduate Research Assistant. (A small tuition remission fee is listed under other direct costs.) An EE graduate student, P. Kshirsagar, has been involved in development of this proposal and would like to use this project as the basis for her thesis. Our electronics engineer, G. Boyd, who is supported by our operating grant, will also participate in the design, fabrication and testing for this project. Fermilab will contribute to the design effort. We are requesting equipment funds each year for chip fabrication through MOSIS and readout electronics to support development. We request travel funds to allow us to make six round trips per year to Fermilab for meetings with collaborating physicists and engineers from Fermilab and BU. Indirect costs are calculated using the OU rate of 45.5% excluding equipment.

Three-year budget, in then-year K$

Institution: Boston University

Item	FY2003	FY2004	FY2005	Total
Other Professionals	0	0	0	0
Graduate Students	\$20.5k	\$12.0k	\$12.6k	\$45.1k
Undergraduate Students	0	0	0	0
Total Salaries and Wages	\$20.5k	\$12.0k	\$12.6k	\$45.1k
Fringe Benefits	0	0	0	0
Total Salaries, Wages and Fringe Benefits	\$20.5k	\$12.0k	\$12.6k	\$45.1k
Equipment	0	0	0	0
Travel	\$1.2k	\$1.2k	\$2.4k	\$4.8k
Materials and Supplies	\$4.5k	\$2.5k	2.5k	\$9.5k
Other direct costs	0	\$14.0k	\$14.0k	\$28.0k
Total direct costs	\$26.2k	\$29.7k	\$31.5k	\$87.4k
Indirect costs	\$16.5k	\$18.7k	\$19.8k	\$55.1k
Total direct and indirect costs	\$42.7k	\$48.4k	\$51.3k	\$142.5k

Institution: University of Oklahoma

Item	FY2003	FY2004	FY2005	Total
Other Professionals	0	0	0	0
Graduate Students	\$12k	\$13k	\$14k	\$39k
Undergraduate Students	0	0	0	0
Total Salaries and Wages	\$12k	\$13k	\$14k	\$39k
Fringe Benefits	\$1k	\$1k	\$1k	\$3k
Total Salaries, Wages and Fringe Benefits	\$13k	\$14k	\$15k	\$42k
Equipment	\$5k	\$10k	\$15k	\$30k
Travel	\$4k	\$4k	\$4k	\$12k
Materials and Supplies	0	0	0	0
Other direct costs	\$1k	\$1k	\$1k	\$3k
Total direct costs	\$23k	\$29k	\$35k	\$87k
Indirect costs	\$8k	\$9k	\$9k	\$26k
Total direct and indirect costs	\$31k	\$38k	\$44k	\$113k