Digital Cavity Resonance Monitor – alternatively way to measure cavity microphonics.*

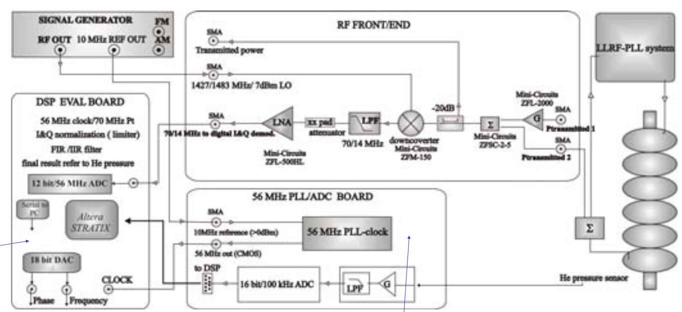
Tomasz Plawski , Kirk Davis, Hai Dong, Curt Hovater, John Musson, Tom Powers

Jefferson Lab, Newport News, Virginia, USA

ABSTRACT

As is well known, mechanical vibrations or microphonics in a cryomodule causes the cavity resonance frequency to change at the vibration frequency. A way to measure the cavity microphonics is to drive the cavity with a Phase Lock Loop (PLL). Measurement of the instantaneous frequency or PLL error signal provides information about the cavity microphonic frequencies. Although the PLL error signal is available directly, precision frequency measurements require additional instrumentation, a Cavity Resonance Monitor – CRM. The analog version of such a device has been successfully used for several cavity tests [1]. In this paper we present a prototype of a Digital Cavity Resonance Monitor designed and built in the last year. The hardware of this instrument consists of an RF downconverter, digital quadrature demodulator and digital processor motherboard (Altera FPGA). The motherboard processes received data and computes frequency changes with a resolution of 0.2 Hz, with a 3 kHz output bandwidth. The results are available in both analog and digital format. These paper discusses the hardware and reports on the test results of the new system.

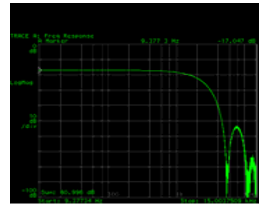
FUNCTIONAL BLOCK DIAGRAM



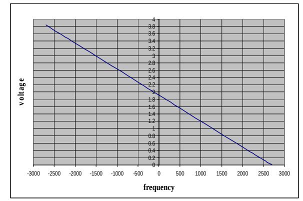
SYSTEM PRINCIPAL

We are using digital quadrature detection of a 1497 MHz cavity probe signal, downconverted to 70 or 14 MHz, then sampled at 56 MHz. In both case I and Q are the result of sampling , however sampling 14 MHz signal instead of 70 MHz provides a better SNR (signal to noise ratio) according to the following formula : $SNR=-20\log(2*\pi*f_t*t_{jitter})dB$ [2] , where f_t is cavity signal and t_{jitter} is a clock jitter. Digital signal processing of I and Q is shown in the next window. The final result is detuning angle and frequency.

DCRM frequency response

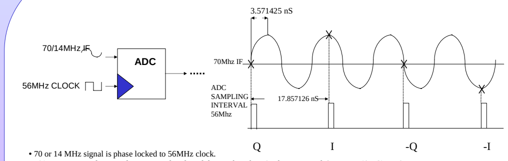


DCRM output characteristic



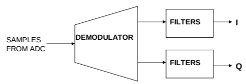
DIGITAL SIGNAL PROCCESSING

STEP 1



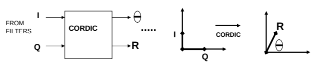
- 70 or 14 MHz signal is phase locked to 56MHz clock.
- 70/14 MHz IF analog signal is converted to digital data with 12 bits Analog to Digital Converter (ADC) at 56 MHz rate.
- Consecutive samples are orthogonal and assigned Q, I,-Q, and –I.
- The sampled signals are digital processed inside Altera FPGA. The processing code is written in VHDL.

STEP 2



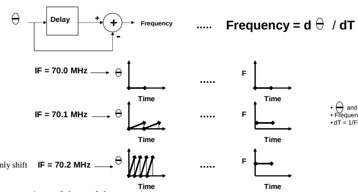
- Demodulator separates samples from ADC into I and Q components.
- The components are filtered to remove signals with frequency above 100 kHz.
- Filtering increases the ADC effective bits by 11

STEP 3



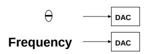
- CORDIC (**CO**ordinate **R**otation **DI**gital **C**omputer) transforms rectangular I and Q components to phase Θ and magnitude **R**
- CORDIC calculates the trigonometric functions of sine, cosine, magnitude and phase (arctangent) to any desired precision.
- CORDIC minimizes the size of electronics circuit (size of FPGA) needed to perform the calculation. The algorithm involves only shift and add. For further information, refer to "A Survey of CORDIC Algorithms for FPGA Based Computer" by Ray Andraka.

STEP 4



- Frequency is rate of change of phase over time.
- Phase change is the difference between two consecutive Θ
- Time is programmed for the frequency range specification.
- For a given dT, the further the IF is from 70MHz, the larger the Frequency value.
- Frequency values are positive or negative for IF that are greater than 70MHz or less than 70MHz respectively

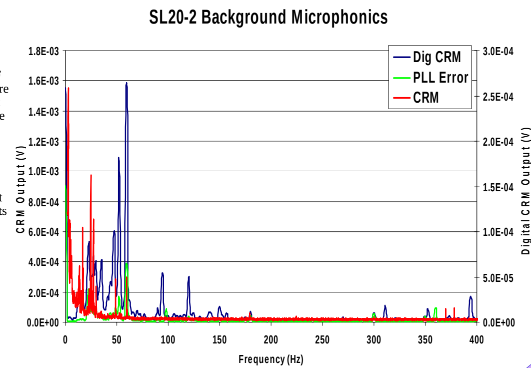
STEP 5



- Θ and Frequency information are output to 18 bits Digital To Analog converters (DAC)
- Frequency resolution = Frequency Range / 2^{18}
- dT = 1/Frequency resolution

RESULT

The digital system was used to measure an operating CEBAF SRF cavity. The results are compared here to an existing analog measurement system, and to a measurement of the PLL error signal. Since the measurements were not taken simultaneously, stochastic components differ between the measurements, but spectral peaks coincide at several known invariant lines (e.g. 27, 30, 59.5). Further tests of the improved instrument are planned.



CONCLUSION

The prototype system was successfully tested with two different type of SC cavities : newer 7-cells installed in FEL, and 5-cell cavities installed in CEBAF South Linac. It is planned to use different RF components and digital-to-analog converters to achieve wider dynamic and frequency range.

ACKNOWLEDGEMENT

Thanks to Curtis Cox at Jefferson Lab for fabrication of the Digital Cavity Resonance Monitor chassis.

REFERENCES

[1] - **MICROPHONICS TESTING OF THE CEBAF UPGRADE 7-CELL CAVITY** K. Davis†, J. Delayen, M. Drury, T. Hiatt, C. Hovater, T. Powers, J. Preble, TJNAF, Newport News, VA 23606, USA , PAC2001

[2] – **UNDERSTAND THE EFFECT OF CLOCK JITTER ABD PHASE NOISE ON SAMPLED SYSTEMS** Brand Brannon, Analog Devices Inc. ,12/07/2004

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