Experience with the New Digital RF Control System at the CESR Storage Ring

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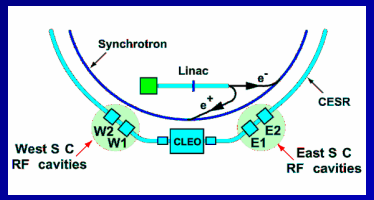
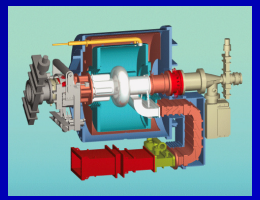
Abstract:

A new digital control system has been developed, providing great flexibility, high computational power and low latency for a wide range of control and data acquisition applications. This system is now installed in the CESR storage ring and stabilizes the vector sum field of two of the superconducting CESR 500 MHz cavities and the output power from the driving klystron. The installed control system includes in-house developed digital and RF hardware, very fast feedback and feedforward control, a state machine for automatic start-up and trip recovery, CW and pulsed mode operation, fast quench detection, and cavity frequency control. Several months of continuous operation have proven high reliability of the system. The achieved field stability surpasses requirements.

CESR RF

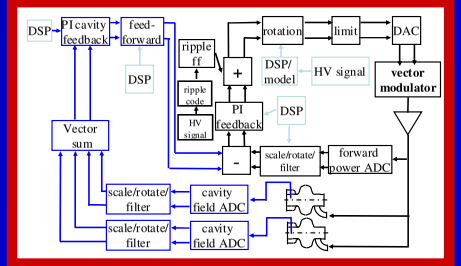




	CESR-c
frequency [MHz]	500
number of cavities	4
cells per cavity	1
R/Q [Ω] per cavity	89
Q_0	1.2 to $1.6 \cdot 10^9$
Q_{ext}	$2 \cdot 10^5$ to $4 \cdot 10^5$
acc. voltage per cavity [MV]	1.9 to 3
required klystron power per cavity [kW]	up to 180
required relative amplitude stability (rms)	< 1 %
required phase stability (rms)	< 0.5°

- Superconducting RF cavities.
- Two cavities are driven by one klystron in parallel.
- Digital LLRF system has been installed for the West Cavities (W1 and W2).
- High beam currents (several 100 mA).
- Low loaded Q.

LLRF Software



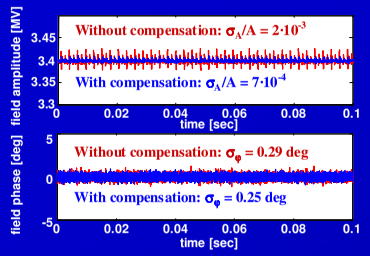
FPGA:

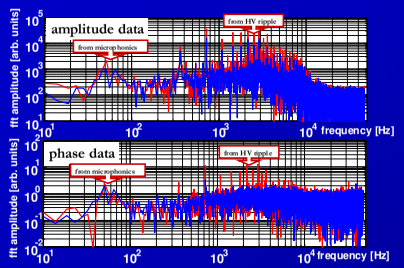
- True vector sum control of the fields of the cavities W1 and W2 (proportional-integral gain cavity loop with reduced bandwidth to avoid feedback at the synchrotron frequency).
- Proportional-integral control loop for the klystron output (several 10 kHz bandwidth).
- Fast klystron high voltage ripple feedforward.

DSP:

- Trip and quench detection.
- State machine with auto-startup, auto-calibration and trip recovery.
- Advanced tuner control (slow and fast piezo-electric).
- Pulsed operation for cavity processing (including feedback loop on vacuum signals to adjust pulse height or pulse length).
- Operation with adjustable klystron high voltage: power demand signal to adjust high voltage, klystron phase shift compensation.
- Data acquisition with ring-buffers.

Results

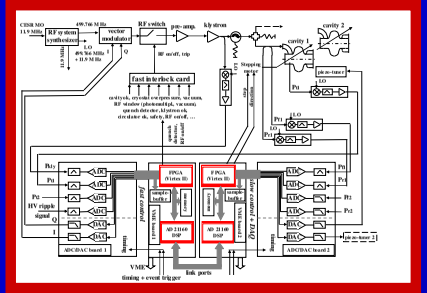




- Digital LLRF system is in operation in CESR since Summer 2004.
- No unplanned downtime has been caused by the LLRF system in the last six months.
- Achieved field stability surpasses requirements.
- Phase fluctuation is dominated by CESR reference noise.
- Klystron high-voltage ripple is the dominating field perturbation. Feedforward compensation proved very effective.

LLRF Hardware

- Very low delay in the control loops.
- Field Programmable Gate Array (FPGA) design combines the speed of an analog system and the flexibility of a digital system.
- High computation power allows advanced control algorithms.
- All boards have been designed in house.
- The controller is designed to stabilize the in-phase (I) and quadrature (Q) component of the cavity field. The RF field signals are converted to an IF frequency of 11.9 MHz and then sampled at a rate of 4x11.9 MHz. Accordingly two subsequent data points describe the I and Q component of the cavity field.
- Generic design: digital boards can be used for a variety of control and data processing applications.

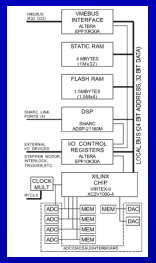


Processor board:

- 4 Mbytes of fast static RAM and 1.5 Mbytes of FLASH memory.
- The DSP is an Analog Devices ADSP-21160N. Four of the six DSP link ports are routed to connectors on the front panel (for connections between RF-DSP boards).
- The XILINX chip is Virtex-II XC2V1000-4. The fast RF control loops and data acquisition control run in this chip.
- Each ADC channel is provided with 2 Mbytes of buffer memory. Incoming data from the ADC are stored in this ring-buffer (1 Msample each).
- A separate memory buffer is provided for the dual functions of storing data directed to the DACs and for a Look-Up Table for feed-forward constants.

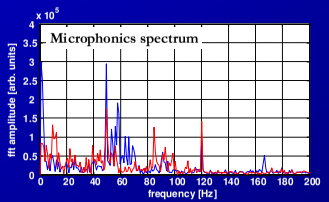
ADC daughter board:

- Four 14-bit 65 MHz analog to digital converters (ADCs) and two 16 bit 50 MHz digital to analog converters (DACs).
- High (74 dB) signal to noise ratio.

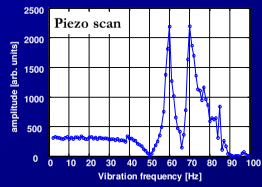


Future work:

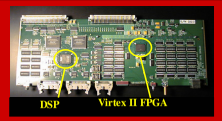
- Improve frequency synthesizer for lower reference noise.
- Work on piezo-based cavity frequency control (microphonics compensation) has started:

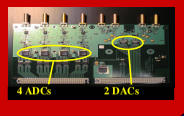


- Microphonics spectrum shows vibrations at relative low frequencies.
- This helps with active microphonics control, but…



- Mechanical resonances of very low frequencies.
- This makes active microphonics control quite difficult (strong phase shift from resonances).
- Need advanced feedback/ feedforward algorithms.





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