Production Testing of the CLEO III Silicon Vertex Detector Hybrid Detector Chain

Eric Reber

Physics Department, Purdue University, West Lafayette, Indiana, 47907

Abstract

Prior to assembling the CLEO III vertex detector, it is necessary to test each of its components before assembly. The Si3 group is testing the electronics chain that will be made into full length ladders and attached to the copper cones in the vertex detector. The testing of the electronics chain is done by using Virtual Instruments (VIs) created with LabVIEW software. My VI has been designed to make the testing process easier and versatile.

Introduction

The CLEO III vertex detector [1,2] is being constructed in order to accommodate the phase III upgrade to the accelerator. One of the major improvements for CLEO III is a new silicon microstrip vertex detector. The Si3 group at Cornell is testing the electronics chains that consist of a silicon detector, flex circuit, and the RC chip with readout electronics (see figure 1). These components will then be shipped to Purdue University where they will be assembled into full ladders and mounted on the end cones for final assembly. The vertex detector will then be ready for installation in the CLEO III detector.

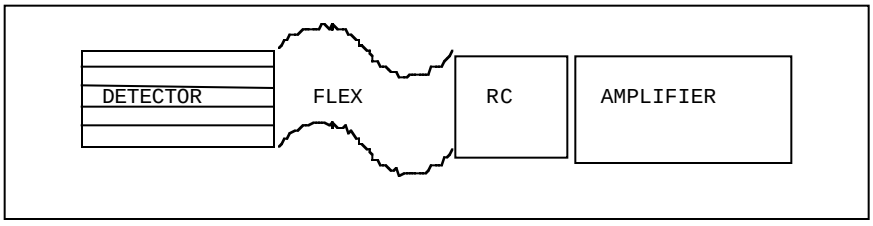

FIGURE 1. The electronics chain that the Si3 group will be assembling and testing.

Testing Requirements

Before we are ready to perform tests on the electronics chain, the chain must be assembled. After the production of the chains is complete, each chain and its 511 channels must be tested. Although each component of the chain has been tested prior to being sent to our lab, it is necessary to test the chain once it has been assembled in case there are problems that arose during production. It is also important to be sure that the readout chip works properly in conjunction with the detector.

Testing Solutions

One of our primary means of testing detectors is controlling and monitoring the current in the detector using LabVIEW [3] programs. The program that our group uses has been designed to perform the entire electronics testing procedure. One of the qualities that makes Lab VIEW so

adaptable is that a program written by someone else can be adopted as part of another program quite easily. All of the testing (see figure 2) of our equipment can be done from a PC in our lab. We use a VME and Data Acquisition Board (DAQ) with a Digital/Analog Converter (DAC) and Analog/Digital Converter (ADC) to allow our VIs to communicate with the electronics that we are testing. The combination of the VME, DAQ, and LabVIEW software has made testing and data acquisition many times easier than with past methods.

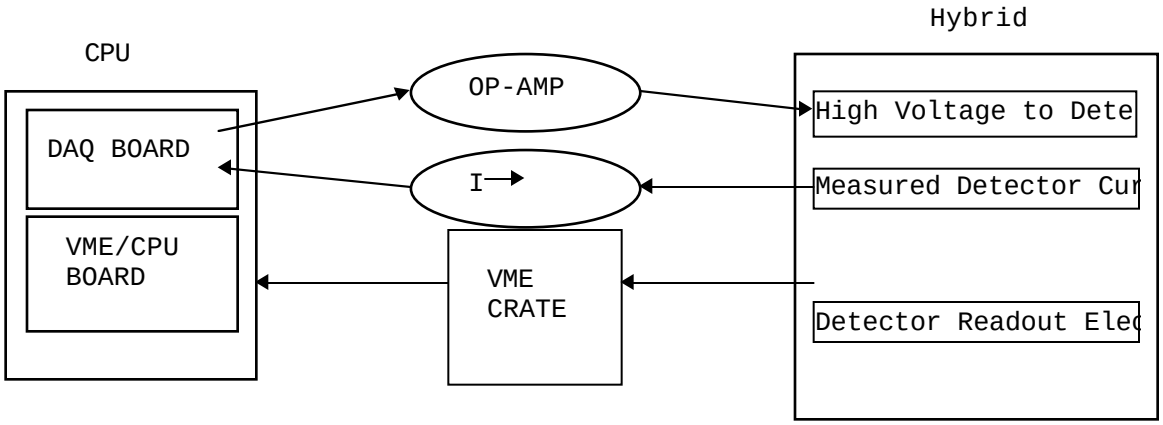

FIGURE 2. The means by which data is acquired during testing.

Specifics

I have built a VI that will make testing the electronics chain much simpler than in previous times. My VI is relatively simple, yet effective in providing the proper means of testing the electronics chain. The VI can be operated from one simple "front panel" (see figure 3), named as such because it appearance and function are similar to that of a mechanical control panel. The front panel is the LabVIEW user interface. The user of the VI can easily manipulate the controls of the VI from the front panel without being concerned with the inner workings of the VI. The front panel allows the user to set the maximum voltage, maximum current, and increment by which the voltage can be changed. There are also indicators located on the front panel that display the current and voltage in the system at any given time.

We have tested the voltages read out by the VI by using a multimeter. The voltages read out by the multimeter agreed with those appearing on the front panel of my VI. Once production is complete, we will be ready to implement the use of my VI. The first step in the testing procedure will be to simply initialize the current in the system to zero. The DAC only supplies a voltage in the range of -5V to +5V. Our voltage requirements are much higher (approximately 100V), so we have incorporated a high voltage Op-Amp into our voltage supply system. By amplifying the voltage from the DAC, we can then ramp up the voltage to the level at which we will perform testing. Throughout the entire testing procedure, the VI will monitor the current, frequently probing for dangerous high currents in the chain. If any high current condition in the chain occurs, the VI will automatically return the current to an acceptable level and alert the user that there had been a change in the current. After the current has been ramped up to the desired level, a sub-VI that has been integrated into my VI will perform tests on the detectors and store the data from those tests. Finally, after the testing of the electronics chain is complete, my VI will ramp the current back down to zero.

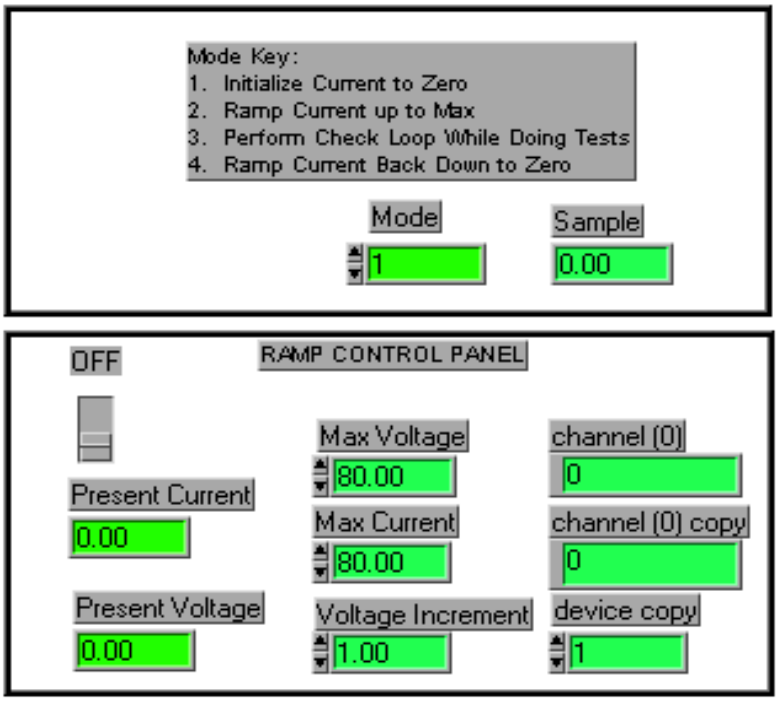

FIGURE 3. The ramp VI which will be incorporated into a larger VI to control the testing of the electronics chains.

Summary

At the present time, our group is still preparing to begin the testing stage of our project. The electronics chains have not yet been constructed, so the full functionality of the VI could not be tested. The VI that will be used for testing the electronics chain is nearly complete. The portion of the VI that performs the ramping and current monitoring has been designed and tested. Further work on the VI will consist of minor debugging. This program, as with all LabVIEW programs, can easily be added to, modified, or incorporated into a larger VI if the need arises. The VI that I have designed also has potential use for and could be easily adapted to applications that may have needs similar to our electronic chain testing.

Acknowledgments

I am pleased to acknowledge Prof. David Cassel and Prof. Nari Mistry, of Cornell University for the work that they have put into promoting this REU Program. I would also like to thank Mr. Naresh Menon, of Purdue University and Mr. Pablo Hopman, of Cornell University for their guidance and assistance in the laboratory during this program. I am also happy to thank Prof. Zbigniew Grabowski, Prof. David Miller, and Prof. Ed Shibata, of Purdue University for making this opportunity available to me. This work was supported by the National Science Foundation grant PHY-9310764 and NSF REU grant PHY-9731882.

References

[1] M.B. Spencer *et al.*, The Design, Performance and Status of the CLEO III Silicon Detector and Low Noise Electronics.
[2] P.I. Hopman *et al.*, Optimization of silicon microstrip detector design for CLEO III.
[3] LabVIEW is a trademark of National Instruments Corporation.