CESR Beam Position Monitors Signal Processing and Synchrotron +24 V Elimination Scheme

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Abstract

The circuitry for the new CESR Beam Position Monitors that prepares and integrates the signals was developed and found to operate correctly. Additionally, the RF system logic cards were modified to accept a 0 to -24 V fault signal.

Introduction

CESR Beam Position Monitors

The current CESR beam position monitors process each monitoring device (button) serially. Therefore, several minutes are required before the position of an entire orbit can be determined. The system under development will continuously process and record the data so that the position of the orbit is continuously updated. Additionally, the new system will be able to take data while the beams are colliding.

The buttons record the position of the beam when a particle packet moves under the button and the charge on the particles induce a charge on the buttons. While the packet moves onto the button a voltage change resulting from the change of charge on the button is read, and while the packet moves off of the button a voltage change in the opposite polarity is read. This process produces a characteristic bipolar pulse whose area is proportional to the distance between the particle packet and the button.

The project concerned with in this paper dealt with producing an integral of this pulse that can be read off by other equipment. The pulse is roughly about 1 ns in length so special considerations needed to be taken in order for this pulse to first be integrated, amplified and extended in time before the resulting integral can be read by other equipment.

Synchrotron +24 V Elimination Scheme

The fault logic levels for the Synchrotron RF system are currently +24 V for not-fault and 0 V for fault. Code states that systems can only be worked on without special precautions when the voltages are no higher than 24 volts. Therefore, a safety hazard exists when some systems run on +24 V and others on -24 V because a net voltage difference of 48 volts exists. It has been decided that the +24 V sources will be eliminated. The fault logic for the Synchrotron RF system is one such source. The 13 cards in this system that have fault inputs needed to be redesigned so that they could take a 0 to -24 V fault logic pulse where -24 V is not-fault and 0 V is fault. (The RF system was originally designed in 1969, before the new code was instated.) Additionally, at each RF station the fault signals needed to be changed so that they are 0 to -24 V.

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The bipolar pulse coming from the buttons is about _100 V and 1ns. However, there was no possible access to the actual pulse, the beam was not on. Therefore, a simulated pulse was needed. Using a short pulse generator a negative pulse of -5 V and 1.5 ns was created. To create the bipolar pulse this pulse had to be inverted then added to itself 1.5 ns later. This was achieved by splitting the signal from the pulser with a coaxial-T adapter, and on one end of the T attaching a short coaxial cable of about 0.75 ns long (3 inches) and grounding the end. This created an electrical ``echo chamber'' where the echoed pulse is inverted and after the pulse travels the rest of the cable length to meet up with the original pulse traveling through the other end of the T it is ~1.5 ns later. This system produced a bipolar pulse of 2 V and 2 ns. The echoed pulse was actually returned in shorter time than 1.5 ns in an effort to shorten the bipolar pulse so that it is more representative of the actual bipolar pulse of 1 ns, however, doing so decreased the amplitude of the pulse to 2 V. (see figure 1)

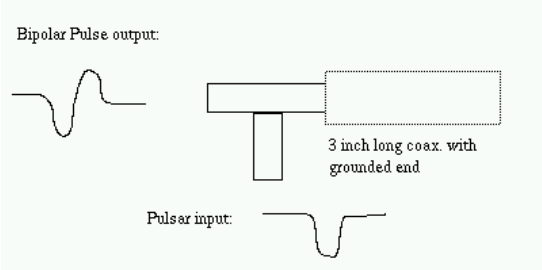

Figure 1: Coax.-T to create bipolar pulse

The net area under the bipolar pulse is zero (equal above and below zero). Therefore, to obtain a usable integral to determine the position of the beam only one-half of the bipolar pulse should be integrated. To do this the two halves of the pulse must be separated so that one-half of the pulse can be isolated and integrated. Using a diode to remove half of the pulse is not possible because even the fastest available diodes are too slow to use with 1 ns pulses that are separated by only 10 ns. Therefore, a different approach must be used. The isolation was accomplished by creating an adder that adds the bipolar pulse to itself delayed by half its length. The adder first splits the pulse, then these two equal pulses travel through two unequal coax. cables (one being about 1 ns longer than the other) and then add together through a three-way 50 ohm coupled coax. split. The overlapping regions when added together cancels each other out (see figure 2). By separating the two halves of the pulse it is possible to isolate and integrate one-half.

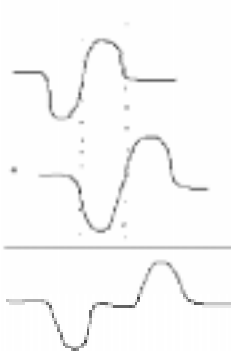

Figure 2: Adding the pulses to isolate one-half of the signal

The integrating circuit itself (see figure 3) takes a negative pulse and while the ECL logic gates are on will integrate the pulse. Then, when the gates are turned off the transistor below the output terminal is turned off thus isolating the RC circuit so that the integral decays off by the time constant RC=10 _s. Fast HFA3102 transistors were used.

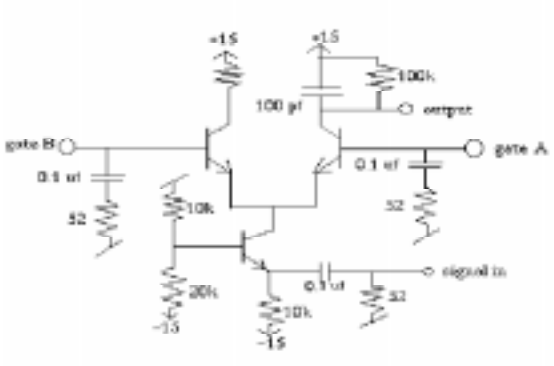

Figure 3: Integrator

To use this integrator with the bipolar pulse the gates must only be on when the negative part of the pulse is fed into the circuit. A MC10198 ECL monostable multivibrator was used to produce the gates. It has a minimum pulse width of 10 ns and a rise time of 2.5 ns. This is not an idea multivibrator for this use but it did work. The rise (and fall) time is as long as the bipolar pulse itself, however, by lining up the ECL logical high (and low) cut-off point with the space between the two separated halves of the bipolar pulse, the integrator is cut-off at the proper moment. If it is deemed necessary the multivibrator can be replaced with one with a faster rise time. The gates can be on long before the bipolar pulse reaches the integrator; nothing is integrated because the distance between the bipolar pulses is longer than the multivibrator pulse width. The gates must be timed with the negative portion of the pulse. The only practical way to accomplish this is with lengths of coaxial cable to delay the gate. RF pulses are quickly absorbed by stray capacitances unless the signal lines are shielded. The circuits themselves also need to be kept as small as possible to also lower any stray capacitance.

In the real device the multivibrator will run off an external trigger that triggers whenever a positron or electron packet moves under the button. Therefore, the bipolar pulse must be timed correctly before it reaches the integrator so that the gate pulses can line up with the negative part of the pulse. For positrons, the negative pulse is first, for electrons, it is second. The method to achieve this is to have a timing mechanism for the gates that will alter the delay time for the pulse to coincide with whichever type of particles may be passing under the button at that time. See Figure 4 for a complete circuit schematic.

Synchrotron +24 V Elimination Scheme

The RF fault logic system consists of 13 cards. For most of the cards changes were only needed to be made to accommodate the not-fault signal to -24 V rather than +24 V. But for the Fault Gate Logic Card an additional change of changing the power supply to the card from +24 V to -24 V was made.

The fault input stages on the cards were modified such that the logic levels out of the fault input stages remains the same so that the rest of the logic on the cards remains the same. Certain other modifications needed to be made such as introducing new power sources (of different voltage levels), switching the polarity of transistors, etc. All modifications have been noted on the circuit diagrams and will be reprinted

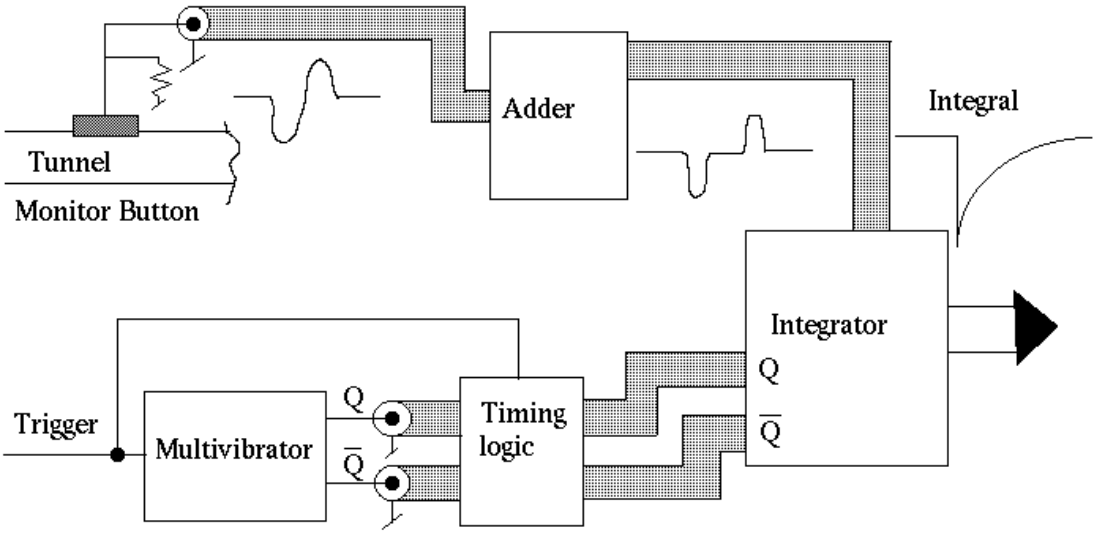

Figure 4. circuit schematic

Conclusions

CESR Beam Position Monitors

The above circuit correctly integrated the small pulse, and the resulting integral was about 10 μs. Long enough so that it is trivial for other equipment to read the integral. A background output of 26 mV exists from the gates without a pulse to integrate, but this is very small and can be calibrated out. The test pulse used was much smaller than the real bipolar pulses and had a maximum integral of about 70 mV. The real pulses will produce integrals much larger than this and the integrator was tested for linearity up to 2.8 V so the circuit is expected to operate correctly for the real bipolar pulses. To further develop this system the circuitry that interprets the integrals and the user interface that will display the information must be developed.

Synchrotron +24 V Elimination Scheme

After modifications the cards were tested and found to operate consistently with the way they did before the modifications. However, the entire system cannot be tested until the modifications to the RF stations have been completed.

Acknowledgments

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