Optimization of RICH Electronics

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Abstract

The Ring Imaging Cherenkov (RICH) Detector provides particle identification for the CLEO III detector at the Cornell Electron Storage Ring (CESR) at Cornell University. The RICH was installed and has been functioning well since August 1999. In order to provide high quality particle identification, the operation of the RICH and its electronics are continually monitored. This summer's research experience was designed to explore the electronics' performance in detail, diagnose any problems that have arisen since installation and develop solutions that will improve the performance and useful lifetime of the RICH.

Introduction to the RICH Detector

The RICH detector is a barrel shaped device in CLEO III located between the Drift Chamber and the Crystal Calorimeter.[2] The beam line runs along the z-axis of the detector. The RICH is 2.5 m long and is located in the region of radius 80-100 cm. The RICH is comprised of three components: a radiator, an expansion volume, and a photon detector.

The actual detection sequence of particle detection goes as follows. A particle formed in the interaction region enters the RICH through a LiF radiator. Because the particle is traveling faster than the speed of light in the radiator medium, it emits a cone of Cherenkov radiation at a fixed angle described by Equation 1 and Figure 1.

$$\cos\theta = \frac{1}{n\beta} \tag{1}$$

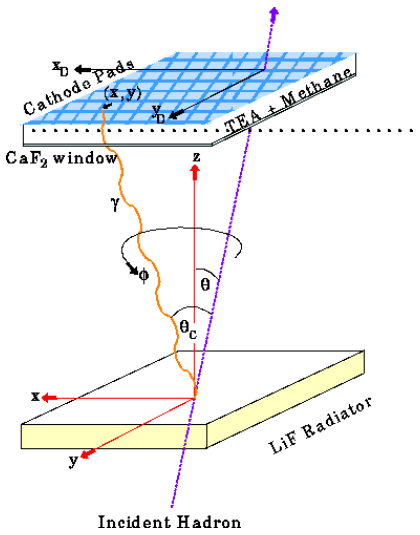

FIGURE 1. A charged particle and its Cherenkov cone passes through the RICH.

Here n is the index of refraction and β is the particle's velocity as a fraction of the speed of light. At angles close to normal incidence most of the light is lost to internal reflection. To prevent these loses the emission surface of 4 of the 14 LiF crystal rings that comprise the radiator layer are not planar, but "sawtooth." [1]

The cone and the incident particle then enter into the expansion volume of pure N_2 gas. The cone is allowed to expand so the distance between photons detected in the next layer is sufficiently large.

The photon detector itself is a multi-wire chamber comprised of a CaF_2 window deposited with metallic traces kept at -1200V, a volume of gas containing a mixture of methane (CH_4) and the photosensitive organic vapor triethylamine (TEA), anode wires kept at +1500V, and a grid of 8.0 x 7.5 mm^2 cathode-pads. A Cherenkov photon that passes through a CaF_2 window is converted into an electron in the gas volume by ionizing a TEA molecule. The photoelectron is accelerated in the electric field between the traces and the anode wires. As the photoelectron collides with other gas molecules, the molecules ionize and more electrons are released. The additional electrons accelerate toward the wires, strike more gas molecules and form an electron avalanche. The avalanche of electrons is deposited on the anode wires, which are capacitively coupled to the cathode pads. The signal from a cathode pad is read out and processed as a single analog channel. Due to the size of the detector, there are 230,400 channels to read out.

Although 23,000 electrons are produced on average by a single photon, this charge is quite localized. The vast majority of the cathode pads should have no charge induced when a particle passes through the detector. To distinguish real signals from fake tracks, the RICH requires low noise electronics to minimize false tracks.[3] A specially designed VA_RICH VLSI chip processes the signal from 64 channels. The chip contains a preamplifier, shaper, and buffer to drive a differential current output pair. Two chips are grouped as a chip-carrier. Five chip-carriers are cabled together into a chain so that their signals are transported to receivers and five analog-to-digital converters. The ADCs are located on data boards in VME crates outside CLEO. There are eight crates, each containing 14-16 data boards. The signal from the analog portion of the data boards is passed to the digital part of the data boards and then to computers.

The digital readout from each channel is between 0 and 4096. To allow for full use of this operating range, the pedestal levels, what the channels read when there are no events in the detector, are approximately 2000. If a channel with a pedestal of 2100 registers 2500 during an event, it is known that $2500 - 2100 = 400$ ADC counts are due to charge induced during the actual event. It is necessary to occasionally record the pedestal values for each channel. This is done approximately every 8 hours, although I only examined data from weekly calibration runs.

The primary focus of my summer's research was electronics. There were three main areas of research: identification and classification of flat chips, exploration of long-term SBUS operating points, and single channel calibration. Each project will be explained in further detail below.

Flat Chips

Flat chips are just what the name implies, chips that appear flat during a small calibration run. A flat chip has an output that is constant for all its channels, independent of the channel input. The channels do not respond individually and all their pedestal values are equal. See Figure 2 for a graphical explanation. Although the existence of flat chips has been known since the beginning, a preliminary study of the long-term behavior of flat chips was undertaken for the first time this summer.

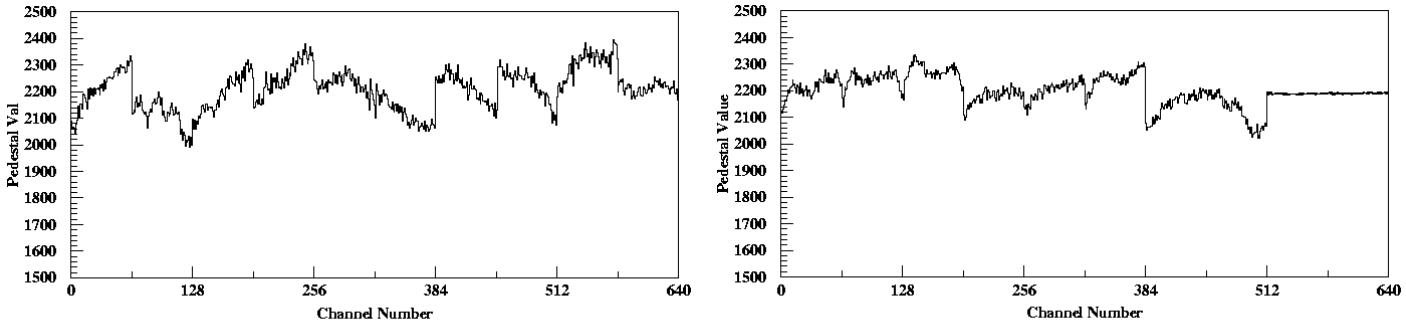

FIGURE 2. The plot on the left shows the pedestal values for a normal chain of 10 chips. The chain on the right has two flat chips. Notice the last 128 channels have the same pedestals.

Flat chips can be identified numerically as well as visually. Examining channels 8-62 of a 64-channel chip, one can calculate the average pedestal value of the chip and its root-mean-square value, where $rms = \sum(pedestal - average)^2$. If the rms is less than ten, the chip is considered flat. A code that calculates the rms for every chip and flags the flat ones already exists.

This summer I wrote new code to identify and flag zig-zag chips. Zig-zag chips are explained visually in Figure 3. This oscillation between two pedestal levels was first noted during initial analysis of flatness. Although the original flat chip code did not flag these chips, such chip behavior is unacceptable. To identify zig-zag chips as well as flat chips, the new code calculates the differences between consecutive channels, finds the average difference, and the rms difference. If the rms is less than five, the chip is flagged. The new code performed better than the existing identification code. When the new code was run on the same small calibration run file as the original code, the new code flagged the same flat chips, as well as the additional zig-zag chips and chips with pedestal values below 100 or above 3900, a region excluded by the original code.

The purpose of this preliminary study of flat chip behavior was to explore the time dependence of flatness. This was done by first identifying the flat chips in a single small calibration run using the new code. Then a shell script looped through all of the small calibration runs to generate graphs of chains containing flagged chips. I visually scanned these graphs, characterized each flat chip's long-term behavior, and created a database for this information. Interestingly, as more was discovered about flat chip behavior, a new

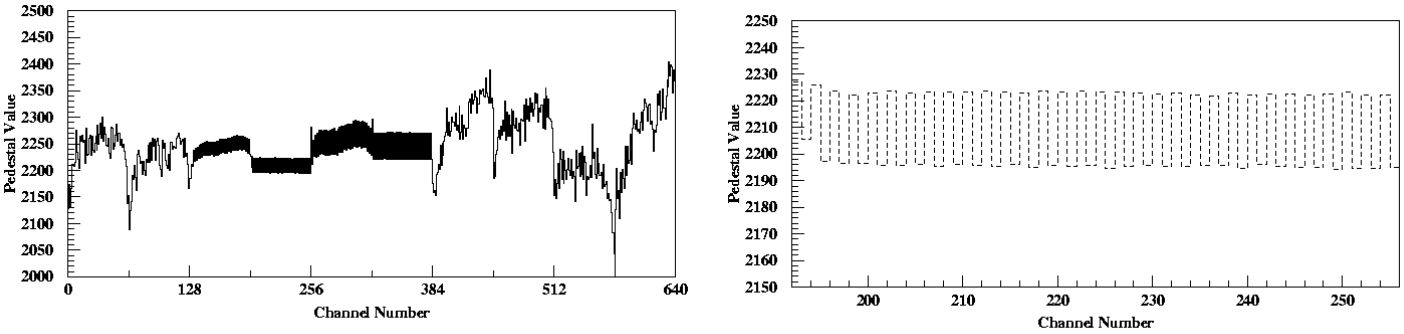

FIGURE 3. The plot on the left shows a chain that was flagged for containing zig-zag chips. The plot on the right zooms in on the fourth chip.

vocabulary became necessary.

Flat chips can be stable, unstable, consistent, or inconsistent. Chips that are stable have pedestal values that remain the same; they do not shift up or down. Because these chips read the same value during the small calibration runs as they do during operation of the detector, they never register hits. Chips with unstable pedestal values may always be flat, but their pedestal values shift up or down without any noticeable pattern. If a chip's pedestal level shifts after a small calibration run, the chip will falsely claim to witness every event, but what it sees will never change. Consistent chips are always flat, while inconsistent chips alternate between flat and working.

In preparation for further study, the new code was run on all the weekly small calibration run data. It is interesting to note that the number of flat chips in each run was approximately 100. I generated files containing the address of each flat chip and its rms value for each small calibration run so that changes in the chips between runs may be more closely studied. Using the current database and these new files, an appropriate plan of action to deal with flat chips will be formed. The operating points of the inconsistent chips will be tweaked in an attempt to return them to working status. Chips that have been consistently flat over the course of several months will probably be masked out of the system.

The investigation of what triggered the onset of flatness or the return to normal pedestal profiles led to the next section, a study of the long-term behavior of the RICH's operating points.

Slow Control Bus (SBUS)

The RICH has a "slow control" system that continually monitors its operation. This system is decoupled from the data-taking portion of the electronics. Although it uses the same voltages and shares the same boards as the read out system, the slow control system has no control over the operation of the VA_RICH chip. The output of the slow control system is a file containing the address of each chain and its operating points. These files are generated every five minutes.

The initial study of the slow control parameters began with a thorough investigation of the temperatures of the ADCs. I looped over all of the SBUS files generated before CESR shut down for the summer to generate graphs of the thermistor values for each ADC like the one found in Figure 4.

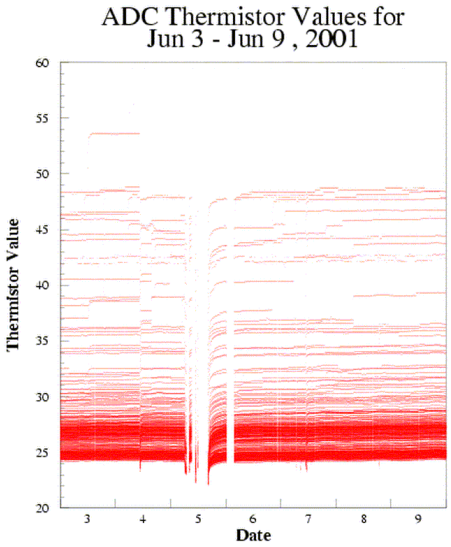

FIGURE 4. This is an example of a normal week for the 360 thermistors. The space on the fifth is due to the usual Tuesday shutdown of CESR.

While the bulk of the thermistors read at 25, there are several that read higher. When examining these higher values, it is also possible to see jumps and drops that do not correspond to the normal operation of the RICH. Because they are thermistor values and not thermometer values, it is possible that the high readings and discontinuities stem from a problem in the electronics. To better understand the nature of this phenomenon I increased the scope of my investigation to include the other relevant voltages and currents. I generated graphs of the vref, ibuf, and temp values of all 360 thermistors during a week. These graphs may be found at http://www.lns.cornell.edu/~deisher/thermistor.html, and a sample may be found in Figure 5.

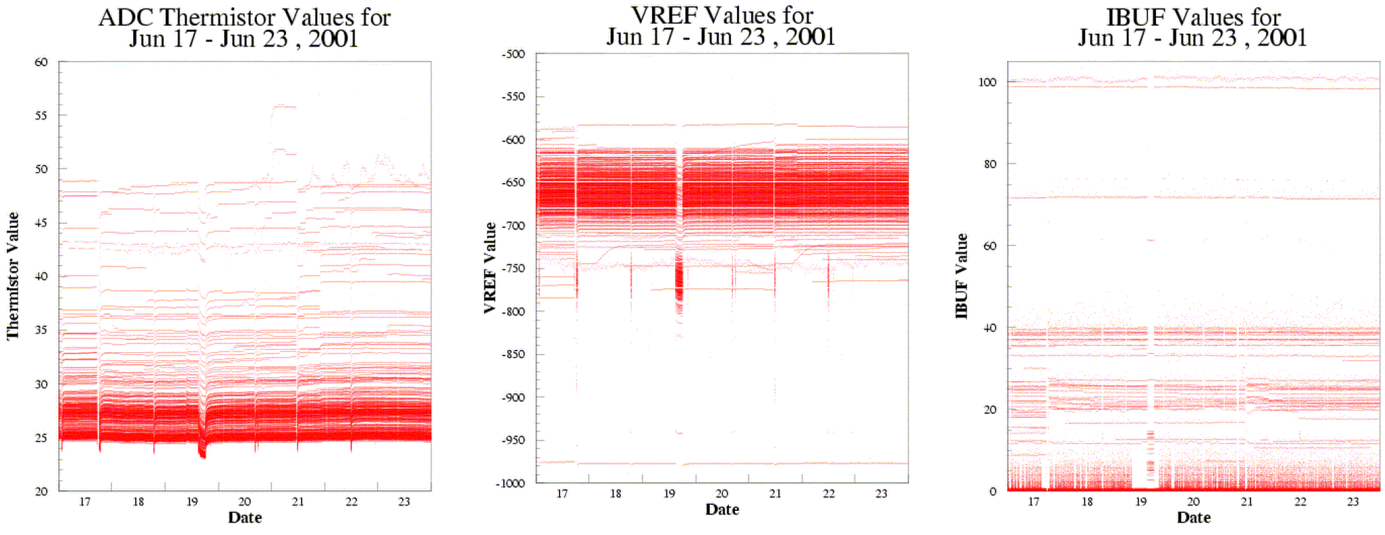

FIGURE 5. This is an example of a normal week for the 360 thermistors. The space on the fifth is due to the usual Tuesday shutdown of CESR.

A comparison of the vref and thermistor plots for the same period strongly suggests that the jumps in thermistor values may correspond to jumps in vref. To localize where this

effect was taking place, I scanned a single day's files for jumps of at least 15 mV in vref. I then extracted the ibuf, vref, vfp, and temp values over a six-week period for all the ADCs flagged by the scan. A sample plot for a single ADC is show in Figure 6.

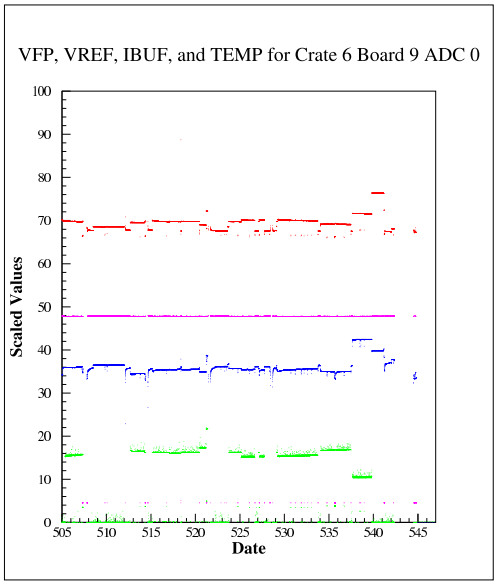

FIGURE 6. The top line is vref. The second line is vfp. The third line is the thermistor value. The bottom line is ibuf. The x-axis values correspond to the number of days since Jan. 1, 2000. Day 505 is equivalent to May 20, 2001.

After studying these plots, we concluded that the high thermistor readings are not indicative of a actual increase in temperature, but rather a change in the operating voltages. Because the vfp values were constant, we can tell that this is not a problem that originated on the boards, but it is an indication of fluctuations on the chip-carrier. These initial plots and studies have given us a greater understanding of the operating points of the detector and will provide direction for further exploration.

Single Channel Calibration

To accurately determine the position of the Cherenkov ring and the center of mass of the particle in the RICH detector it is necessary to know how much charge has been induced on each cathode pad. However, no one physically counts the number of electrons in the detector. As previously mentioned, the analog signal coming from the detector is converted into a digital signal (possible values 0-4096) by an ADC in the crates. The relationship between the charge X induced on the cathode pad and the digital signal $ADC(X)$ should be proportional, but the functional relation has not yet been completely characterized for all channels in the detector. Single channel calibration is a process that has been designed to define the $ADC(X)$ function for each channel. This summer was the first time that such a calibration run has taken place.

During a single channel calibration, charge is injected into the system through a second entrance into the electronics, not by pulsing the anode wires. The gain curve of a channel is traced out by plotting the ADC output versus the injected charge. There were 9 different values of injected charged used in this initial test of the system (400, 800, 1200, 1600, 2000,

2400, 2800, 3200, 3600). Each channel was actually pulsed 50 different times at each X value. The average ADC response was then curve fit to Equation 2. Figure 7 shows a sample curve fit.

$$ADC(X) = Pedestal + Saturation * \tanh((X - Offset) * \frac{Gain}{Saturation}) \quad (2)$$

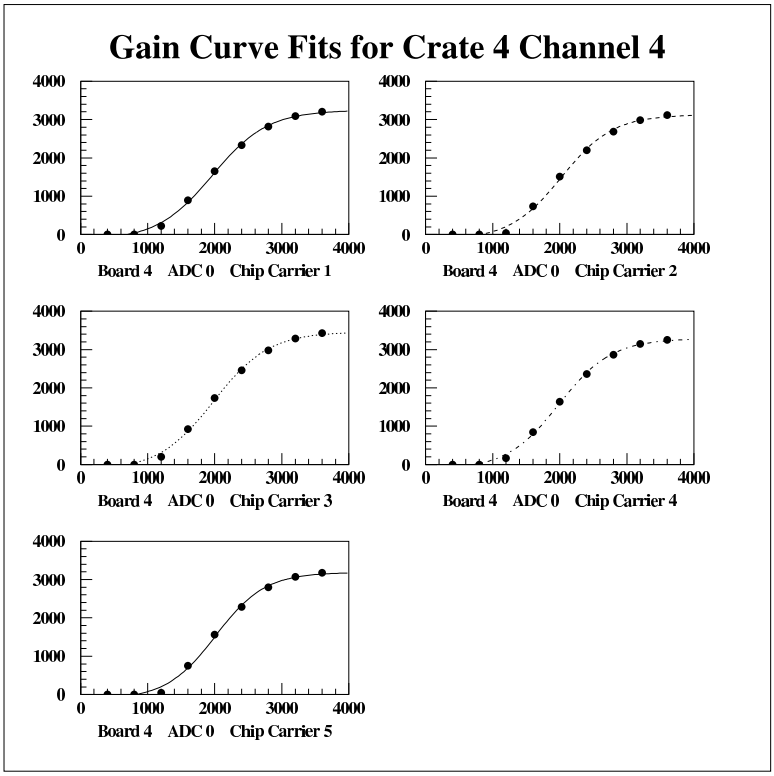

FIGURE 7. A plot of $ADC(X)$ vs. X (points) and the hyperbolic tangent fit (curve) for five individual readout channels of a single ADC.

Pedestal refers to the vertical shift of the hyperbolic tangent function, normally centered at (0,0), while $offset$ refers to the horizontal shift. *Saturation* describes the attainable ADC values, where $2 * Saturation$ is the full range of the hyperbolic tangent function. *Gain* is the slope of the function near its center. When X is approximately equal to $offset$, $Y = |X - Offset| * \frac{Gain}{Saturation} << 1$. Since $\tanh(Y) \approx Y$ for small values of Y, we can approximate the gain curve in this region by $ADC(X) = Pedestal + (X - Offset) * Gain$. *Gain* is then obviously the slope of the equation in this region. There is already room in the memory for these parameters to be stored for each channel, but currently the relationship is assumed to be linear. The initial curve fits have shown that these parameters are pretty uniform for most of the channels. See Figure 8 for histograms of the four parameters. There are a few channels with parameters that are not clustered around the average, but that number is consistent with the number of low gain channels measured previously.

There are several reasons why the shape of the gain curve is quite important. Given an ADC value and the gain curve, one can more accurately determine how much charge was actually induced on the cathode pad. Any tool that can be used to better understand

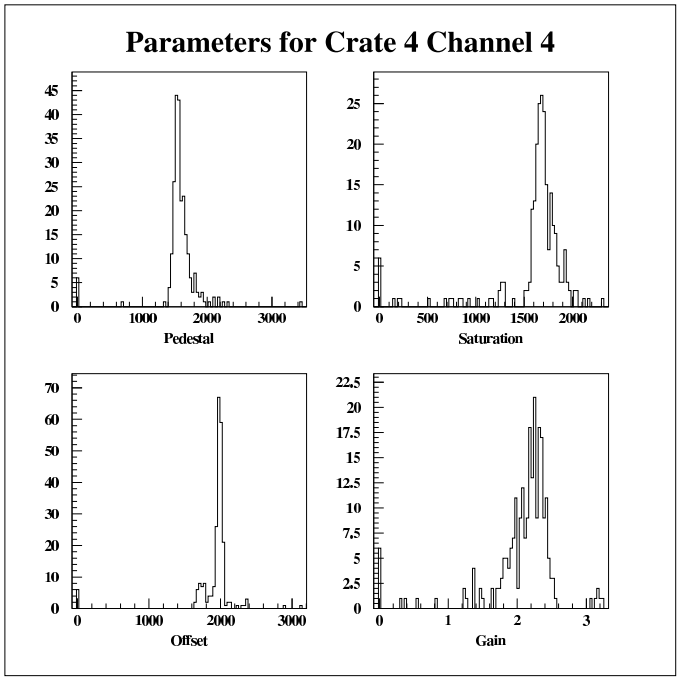

FIGURE 8. Each crate used during the single channel calibration test had 210 channels pulsed. Here is a histogram of the four parameter values for a sample crate.

what actually happened in the detector is, of course, a good thing. While it is obvious that there is a definite upper limit to the ADC value (4096), initial results have shown that the $pedestal + saturation$ value for a given channel is much lower than that. Understanding saturation is important in the reconstruction of the tracks of charged particles. As a charged particle passes through the RICH, it may saturate twenty channels. If the gain curve is well known for those channels, the ADC readout, which looks like a top hat, can then be traced back to the actual charge induced on each cathode pad, which will have a more peaked profile. If we can even just barely make out the peak, then we can more accurately locate the track position by using the center of mass. A single channel calibration performed on a regular basis may be a useful tool to diagnose dying chips. If the gain of the curve decreases, it may be a sign that the channel is part of a chip that is dying. The operating voltage of the chip may then be adjusted.

This summer the single channel calibrations were performed for the first time on a small number of test channel. I wrote software to process the information from this initial test of all the channel fours in five of the eight crates. A macro written for the Physics Analysis Workstation (PAW) was used to fit the individual gain curves. The location of each pulsed channel and its four parameters $(pedestal, offset, saturation, gain)$ were printed to a file. The code written this summer will be modified for use during the full single channel calibrations which will be regularly scheduled starting this fall.

Summary and Future Direction

Significant progress was made on each of the three projects this summer. The classification of flat chips, when combined with further study of their time evolution, will enable informed decisions about the fate of flat chips to be made. The graphical display of the

SBUS operating points and the software developed to scan for irregularities will continue to be useful when analyzing RICH electronic performance. The software developed for the single channel calibration will be used this fall to improve particle identification and track reconstruction.

Acknowledgments

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References

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2. R.J. Mountain et al., Nucl. Instr. and Meth. A 443 (1999) 77-86
3. Further detail about the electronics may be found at the Syracuse University Experimental Particle Physics Group's web page at http://www.phy.syr.edu/research/elementary_particles/experimental/rich_elec.html