Optimization of RICH Electronics Peformance

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Abstract

In order to increase the efficiency of RICH electronics, it is necessary to closely monitor their behavior. This monitoring involves the use of tools such as plots and analysis programs to detect, study, and diagnose unusual behavior. My research this summer focused on creating such monitoring plots and programs and using them to conduct studies into the nature of noise and bad chips found in the RICH detector. Furthermore, I assisted in the setup of a RICH data acquisition testing system that will be used in the future to test RICH electronics and diagnose possible problems with the electronics setup.

Introduction

Since the installation of the RICH detector in 1999, RICH electronics performance has been continuously monitored, and several studies concerning electronics optimization have been carried out. This continuous monitoring has been necessary due to the large-scale nature of RICH electronics and the low-noise requirement for the RICH detector. By observing RICH electronics behavior, the goal is to minimize the occurrence of unwanted phenomena that is statistically bound to occur in any large-scale electronics system and to keep an eye on noise levels in the detector.

Through previous observation of RICH electronics behavior, two potenially related problems have been detected. The first of these problems involves the appearance of flat chips, which are bad chips that occur during small calibration runs. The other problem involves the appearance of white boxes, which are bad chip that occur during data-taking. The goal of my studies this summer was to investigate the behavior of these chips and explore the possibility of a correlation between the two. Furthermore, the working hypothesis that high noise levels play a part in the creation of flat chips was investigated, and the RICH data acquisition test stand was setup.

Time Dependence of Flat Chips

Flat chips are defined mathematically as those chips with an rms value of less than 10, where rms is determined by the following equation:

$$rms = \sqrt{\sum \frac{(pedestal - average)^2}{\#\ of\ channels}} \tag{1}$$

Graphically, flat chips can be identified as those chips whose pedestal plots for small calibration runs resemble flat lines, as opposed to the jagged lines that characterize the pedestal plots of good chips (Fig. 1). These flat lines indicate that each of the chip's 64 channels are reading in approximately the same pedestal value during the calibration run.

Since the data from flat chips is unphysical, it must be ignored, and the usable data size for the RICH detector is decreased.

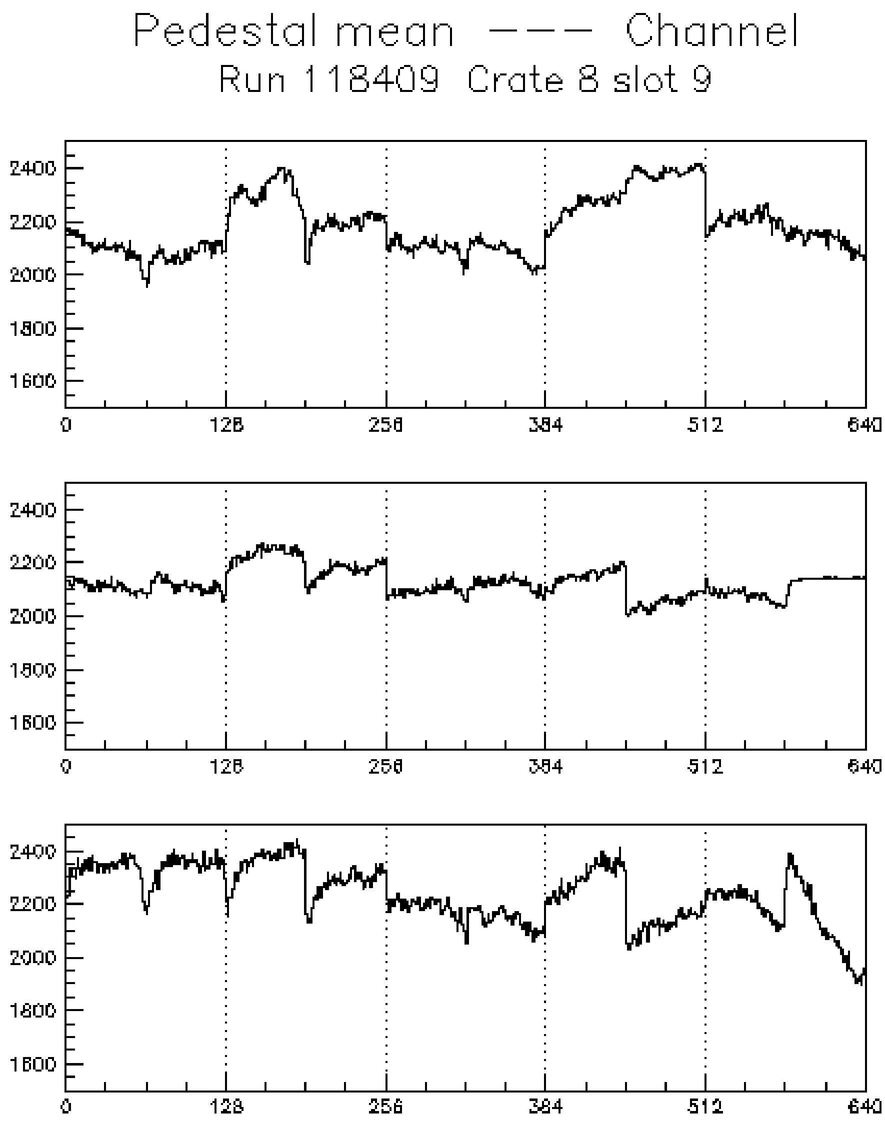

FIGURE 1. This is a typical pedestal plot for a board with three chain consisting of 5 chip carriers each, with each chip carrier containing two chips. In chip carrier 5 of the middle chain, the second chip is flat.

Approximately 4% of all chips in the RICH detector exhibit signs of flatness, and the average number of flat chips found in each small calibration run is steadily increasing. Unfortunately, the cause of flatness has been difficult to determine. This is due, in part, to the inconsistency of flat chips over time[1]. Chips may be flat for several runs, return to working status for awhile, and then become flat once more (Fig. 2). This inconsistency is not the rule, however, as there are also a number of chips that appear to be permanently flat. While the fluctuation in flatness provides hope that some flat chips may be repaired, it makes the cause of flat chips difficult to diagnose. Furthermore, it presents the dilemna as to whether or not event hits recorded on flat chips are to be believed. It is possible that good chips become flat or flat chips become good between calibration runs and actual data-taking.

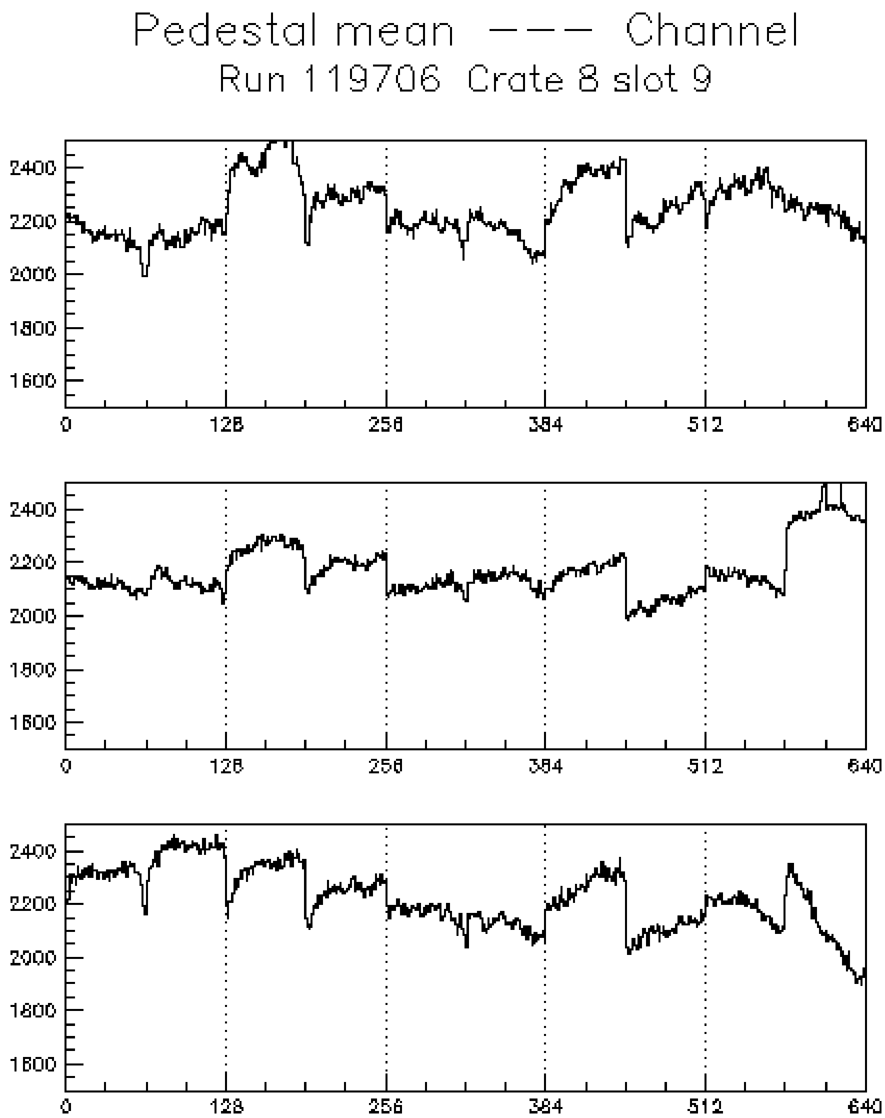

FIGURE 2. This is a pedestal plot for the same 3 chains as Figure 1, but taken during a later calibration run. As you can see, the flat chip from Figure 1 now appears to be functioning properly.

In order to gain a better understanding of the behavior of flat chips over time, I first created a program to loop over the data for various runs from the previous two years and flag all flat chips. Once this was done, I used the data to categorize flat chips into two categories: consistent and inconsistent. Consistent chips were those that were consistently flat throughout all runs and inconsistent chips were those whose status fluctuated. Approximately half of the flat chips in the RICH detector were found to be consistently flat, while the other half were found to be inconsistent. The list of consistent flat chips was then used to create a minimal list of permanent flat chips that could be removed from the database. By removing these chips from the database, disk space can be reduced without loss of usable data.

Noise and its Relationship to Flat Chips

While the reduction of unusable data size might be useful, it would be preferable to increase the amount of usable data by recovering the flat chips. To do this, the cause of flat chips must first be determined. Currently, the working hypothesis is that flatness is the result of a condition frequently found in CMOS devices known as latch-up. Inside each CMOS device is an SCR (Silicon Controlled Rectifier) that is comprised of three terminal components: anode, cathode, and gate. When the small current injected by the gate input exceeds a predefined trigger value, current is conducted between anode and cathode, shorting the device supply. This results in a large current draw between anode and cathode, damaging, and possibly destroying, the device. Latch-up can be caused by either a high current input at the gate or a high voltage applied across the anode and cathode. Either of these latch-up conditions could result from high levels of noise in the RICH detector, which might be responsible for inducing latch-up in flat chips.[2].

In order to explore the possibility that flat chips are a result of latch-up, I created a script to generate and automatically update a RICH small calibration monitoring webpage. By doing so, the relationship between flatness and noise could be studied. The script is comprised of several different elements, each playing a part in the generation of the webpage. A C++ program first communicates with the database and obtains pedestal constants and other run information and creates histograms. A plotting program called PAW is then called to load and plot these histograms. Once this is done, the shell script creates a directory structure for the webpage and generates or updates the necessary HTML files. The webpage contains plots for calibration runs dating back approximately one year and is automatically updated twice each day to include plots for new runs.

For each run several plots are generated. There are three statistical plots that convey the averages and spreads of pedestal values, total noise, and incoherent noise for the entire detector (Fig. 3). These plots are useful in representing global shifts in overall noise or pedestal levels in the detector. A plot depicting the geometrical distribution of both noise and flat chips in the detector is also available so that noise can be monitored on a more localized level, and the correlation between noise and flat chips can be visually analyzed (Fig. 4). By looking at a number of these plots, it can be seen that there may be some correlation between high noise levels and flat chips, but not as much as one would expect if noise were the sole factor in the occurrence of flatness. The final series of plots appearing on the webpage compare the time-dependence of flat chips with the time-dependence of noisy chips for each individual chamber (Fig. 5). Much the same as with the plots depticting the geometrical distribution of noise and flat chips, these time-dependence plots exhibit low levels of correlation between noise and flatness. Due to the inconclusive nature of these results, further study into the relationship between noise and flatness is necessary.

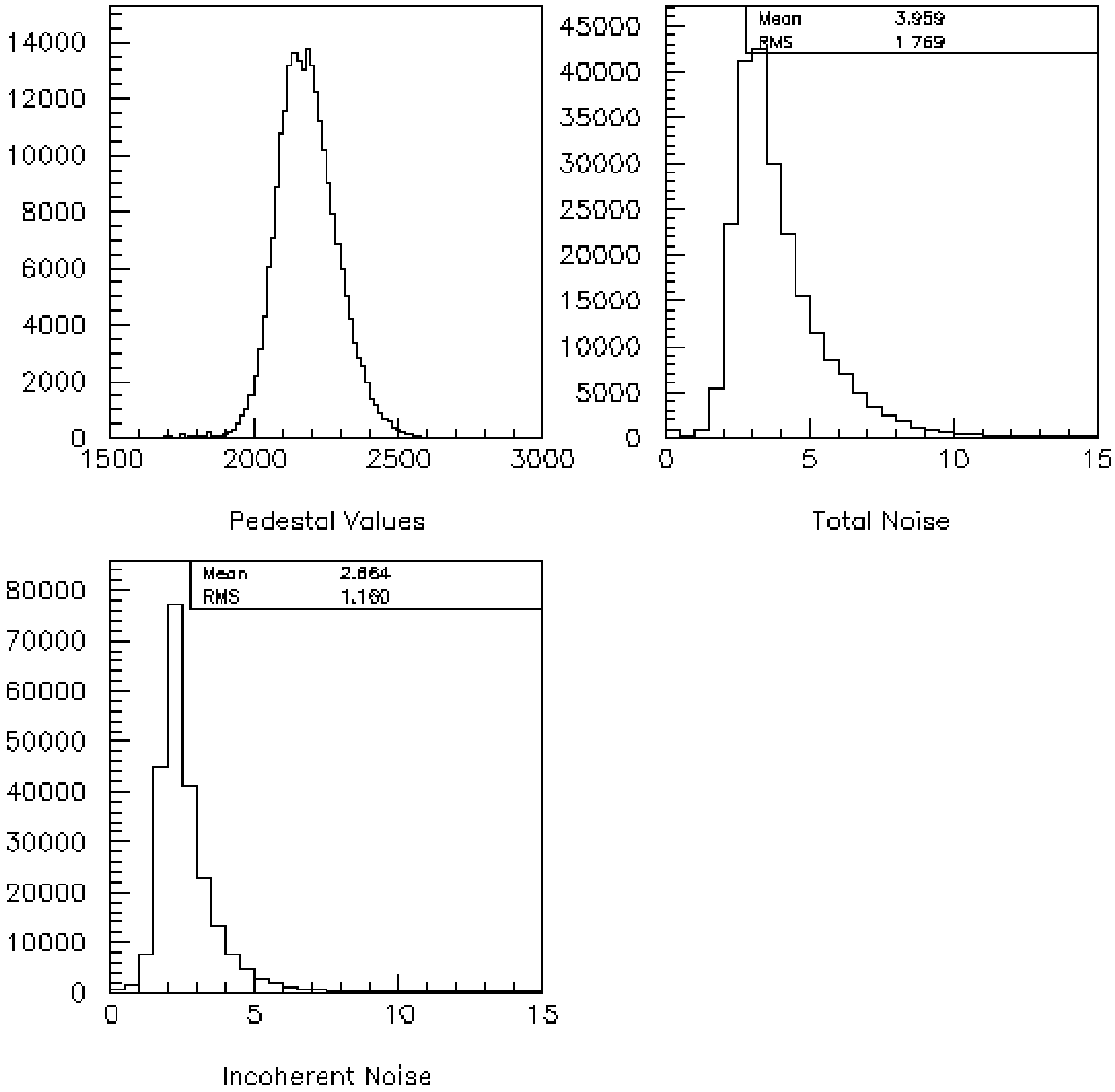

FIGURE 3. These are typical histogram plots for pedestal values, total noise, and incoherent noise in the RICH detector

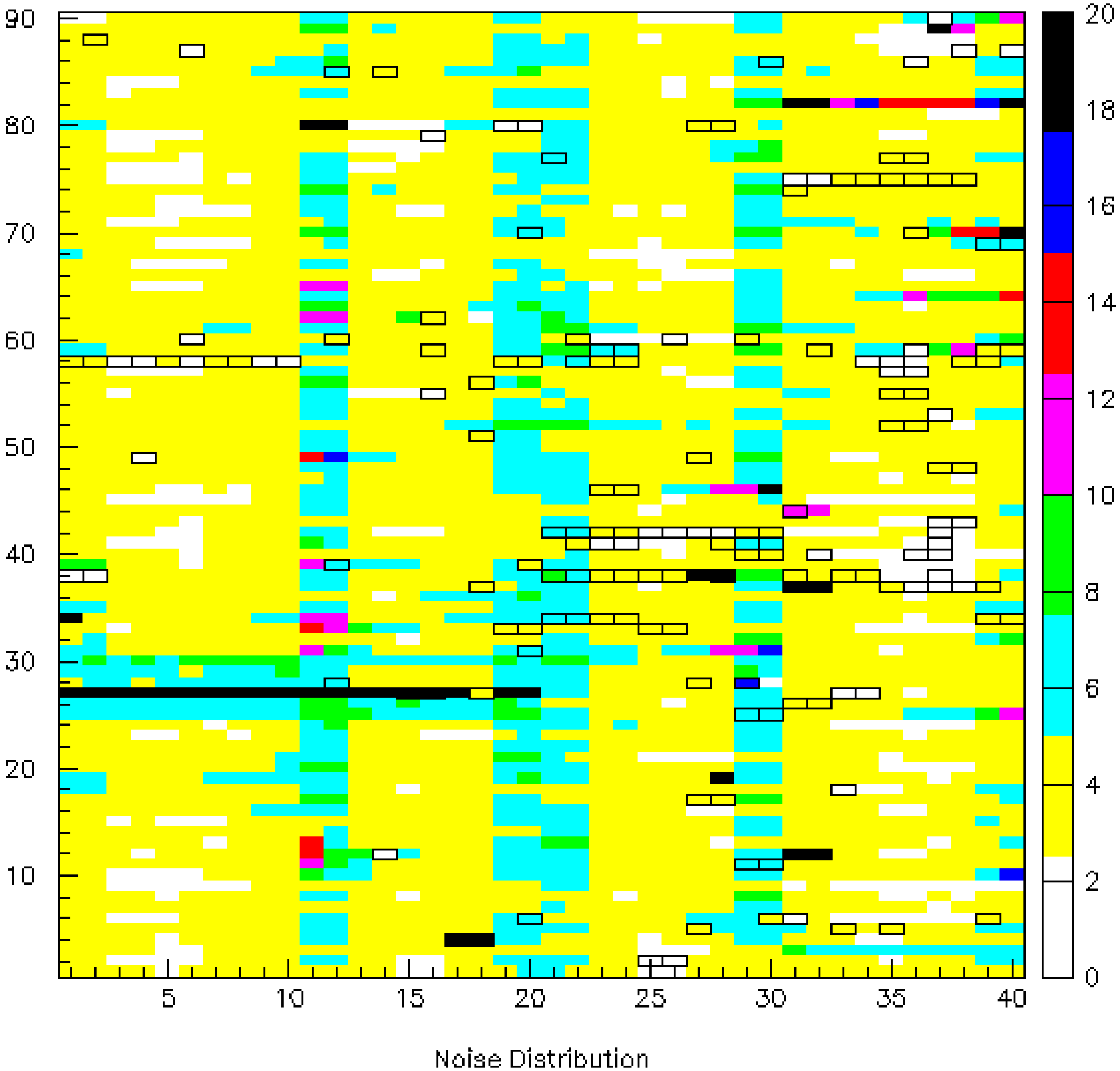

FIGURE 4. Geometrical distribution of total noise and flat chips. Noise levels are represented by a color map, and flat boxes are represented by black boxes

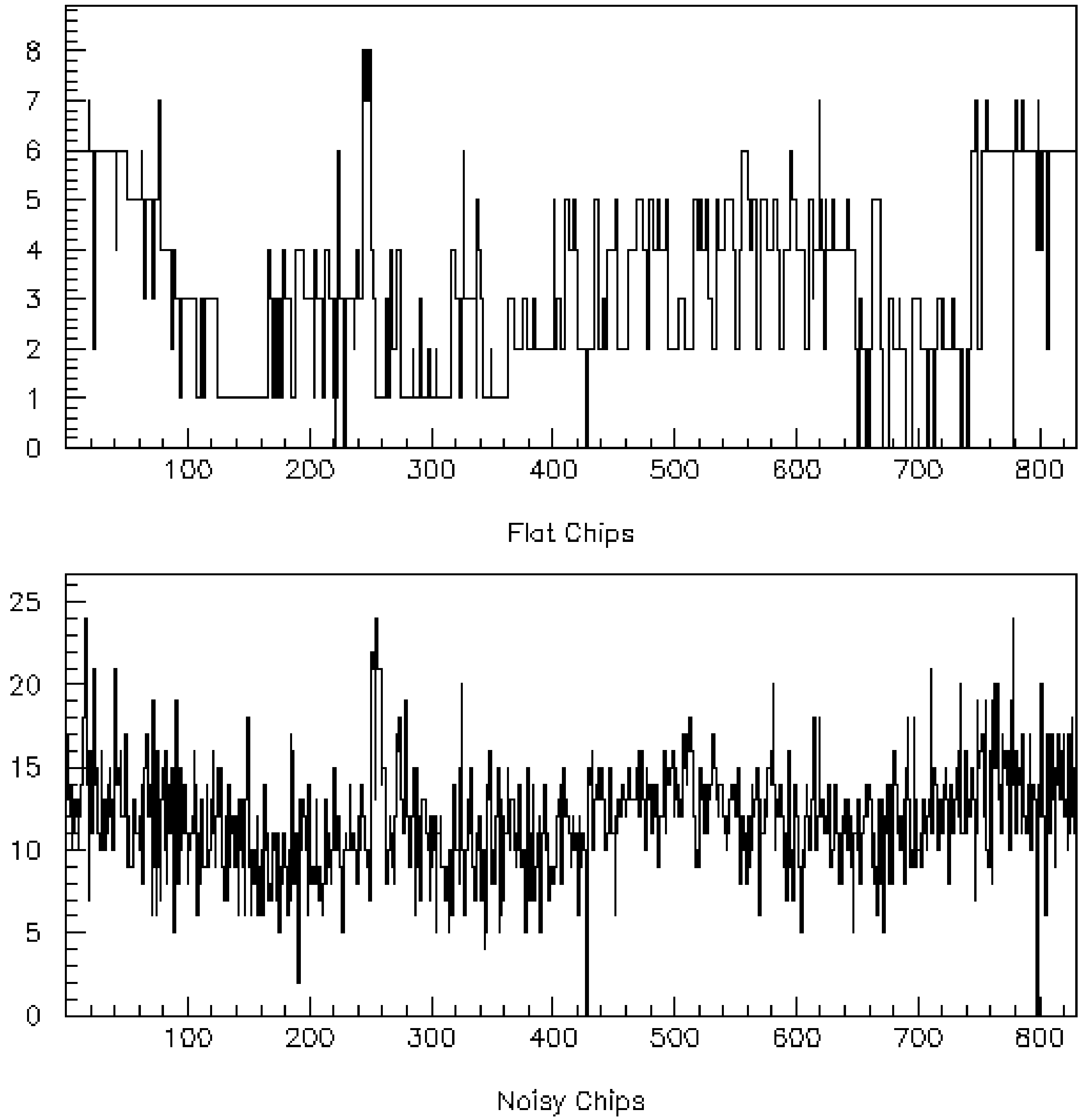

FIGURE 5. The top plot depicts the number of flat chips in chamber 12 over the course of around 850 runs. The bottom plot depicts the number of chips with noise values greater than 6 over the course of the same runs.

Correlation Between Flat Chips and White Boxes

During data-taking, ADC values are read in by each channel. A digital signal processor (DSP) mounted on each digital board then subtracts the previously recorded pedestal value for each channel from this measured ADC value in order to determine if the channel has recorded a hit. When the difference between ADC value and pedestal value is greater than 5 σ, the channel shows up as having received a hit on the event display. If a channel's pedestal value changes more than 5 σ between the small calibration run and data-taking, then the DSP will believe that the channel has recorded a hit. Chips for which a significant percentage of their channels record these faulty event hits are referred to as white boxes. This summer I conducted an investigation into the behavior of white boxes with the goal of better understanding the cause of white boxes and their possible connection to flat chips.

In order to carry out my investigation, I looked through numerous data-taking runs on the event display and looked for a pattern in the occurrence of white boxes. What I found was a seemingly random distribution of white boxes that constantly shifted between each event. A small percentage of faulty hits corresponded to permanent white boxes that remained constant throughout entire runs, and a somewhat larger percentage corresponded to white boxes that disappeared and reappeared regularly in the some location. Of the permanent white boxes, all were present at the beginning of each run; no permanent white boxes appeared in the middle of a run. If a larger percentage of white boxes exhibited this behavior, it might be possible to attribute the cause of white boxes to initialization, but the small percentage makes the study inconclusive.

In addition to studying the time frame for the creation of white boxes, I investigated the possible relationship between white boxes and flat chips. An already existing C++ program was modified in order to generate a plot of the geometrical distribution of both white boxes and flat chips for individual events (Fig. 6). From this plot, it is evident that over half of the white boxes correspond to chips that were flat during the preceding small calibration run. Since flat chips comprise a small percentage of the total chips in the RICH detector, but comprise a significant percentage of white boxes, it would seem that there might indeed be some sort of correlation between flat chips and white boxes. This indicates that flat chips may be more susceptible to pedestal shifts than normal chips. If this is indeed the case, it lends credence to the hypothesis that latch-up is the cause of flatness, as shifting pedestals can be explained by the high current draws that are experienced during latch-up.

RICH DAQ Test Setup

Whenever problems occurs in the RICH electronic setup, or if studies into phenomena such as flatness are being conducted, it is desirable to have a RICH data acquisition test setup with which to test and diagnose the electronics. For this reason, part of my project focused on getting the RICH DAQ test setup up and running.

In order to get the system running, work with both hardware and software elements was necessary. To begin the process of setup, a RICH analog board was connected to a digital RICH board housed in the RICH test crate. Once this was done, I had to learn to use the Session Manager program to take sample data runs. Unfortunately, the first few

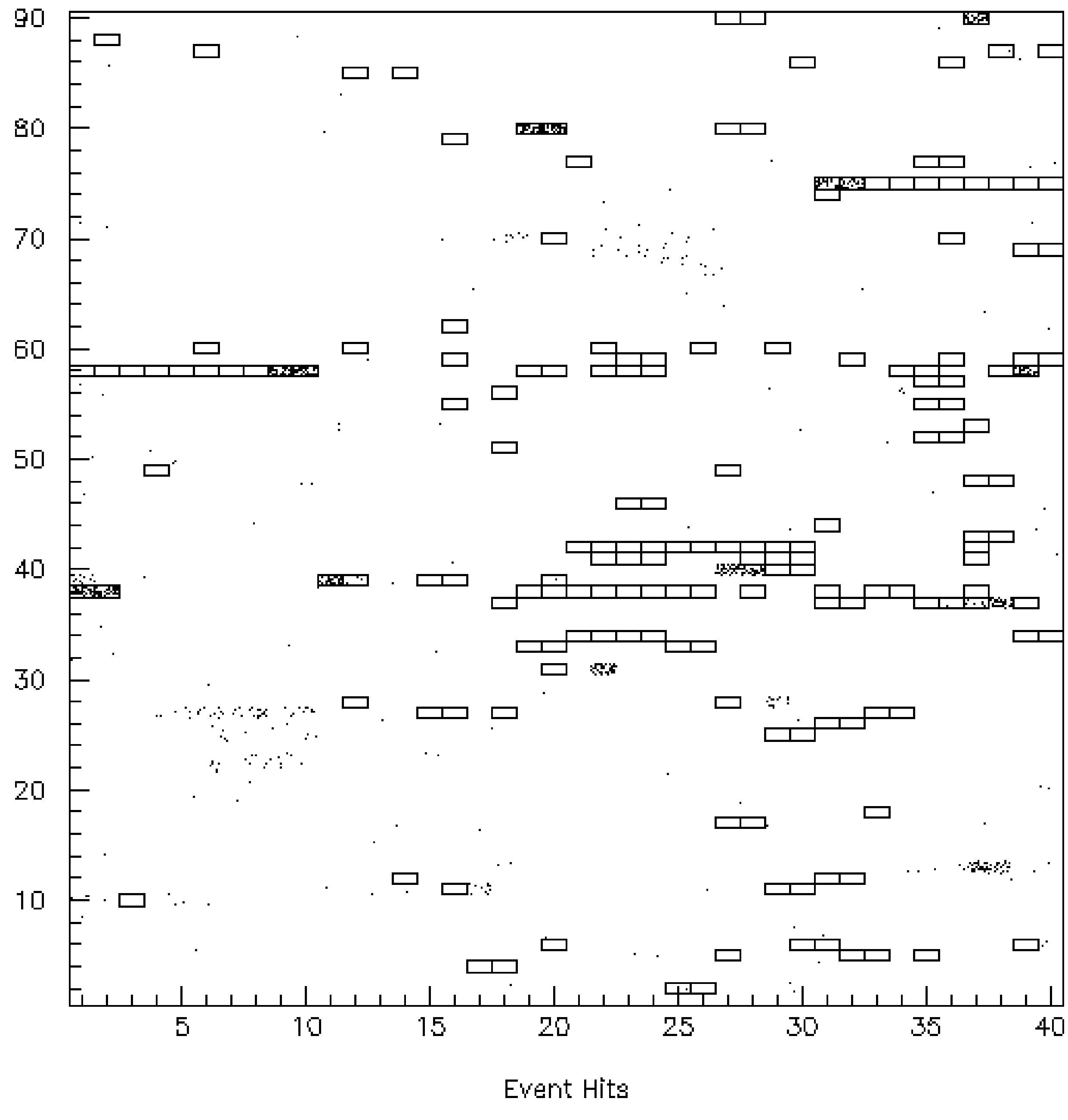

FIGURE 6. Geometrical distribution of 'fake' hits and flat chips in the RICH detector. Black points correspond to 'fake' hits and black boxes correspond to flat chips.

attempted runs indicated that something was wrong with the setup, as the pedestal values were flatlined. I attempted to solve the problem by updating the VME and sequencer chips on the digital board and modifying the plus and minus 2 operating voltage constants for both the digital and analog boards, but with no success. Other solutions, such as changing the cables connecting the digital and analog boards, also failed. Only when a different digital board was installed did it become apparent that the original digital board was faulty and had been causing the unusual behavior.

Once this was done, I moved on to the software portion of the project. This involved some debugging and modification of the small calibration mode for the Run Manager GUI within the Session Manager in order to allow for a set run size of 100 events to be taken. I also attempted to add flash mode to the Run Manager GUI, but with little success. Currently, the RICH DAQ test setup is operational and ready to begin attempts at recreating flatness.

Results and Conclusions

Over the course of my research, various tools for monitoring the performance of RICH electronics were created, and further progress was made in the study of both flat chips and white boxes. A minimal list of permanent flat chips was compiled, and the approximate ratio of consistent flat chips to inconsistent flat chips was determined. An investigation into the correlation between noise and flat chips proved inconclusive, as did the investigation into whether white boxes are caused by something during beam initialization or by some phenomena occurring in the middle of a run. There was some evidence, however, that a correspondence between flat chips and white boxes might exist, which would suggest that flat chips are more susceptible to pedestal fluctuations. This, in turn, supports the working hypothesis that latch-up is the cause of flat chips. Finally, the RICH DAQ test setup was brought to working status and is now available for assistance in investigating the cause of flatness.

Several possibilities exist for further research into the behavior of RICH electronics. The RICH DAQ test setup can now be used to recreate flatness in the test board, which would provide a good idea as to its cause. Further investigation into the nature of white boxes should prove useful in determining when they initially occur and if they are indeed the result of pedestal shifts. If conclusive evidence can be found, then the cause of white boxes can be more easily diagnosed, and perhaps steps could be taken to increase the efficiency of the RICH electronics by minimizing their occurrence.

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Footnotes and References

1. A. Deisher. Optimization of RICH Electronics. (Paper from previous REU student. This paper may be accessed online at www.lns.cornell.edu/~deisher.)
2. Further information concerning latch-up can be found at www.thermokeytek.com/cr/test_methods.htm.