CMS Silicon Pixel Detector Calibration

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The Compact Muon Solenoid (CMS) pixel group at Cornell University is building a silicon pixel detector test station that will model the detection and data acquisition system designed for the CMS experiment at the Large Hardron Collider (LHC) at CERN. With parts of the apparatus already functional, we have begun to understand and optimize the detector's programmable settings, called DACs, that tune its performance. The success of these optimizations has been quantified by performing various calibrations, also being developed here, that will also be used at the LHC to ensure that the pixel detector is working properly and taking the most accurate data possible.

I. INTRODUCTION

The Compact Muon Solenoid (CMS) general purpose detector at the Large Hadron Collider (LHC) at CERN will be exposed to proton-proton collisions happening at a 14TeV center of mass energy [1]. The silicon pixel detector, the innermost tracking device, will provide a precise track origin by weighting the position of activated detector segments, or pixels, with respect to the magnitude of ionization caused by a passing charged particle. The detector will consist of ∼66 million pixels, separated into groups of 4160 that are mounted onto Read Out Chips (ROCs), which are in turn separated into barrel layers and endcaps that encircle the beam pipe and interaction point [2–4].

In order to activate, or "hit", a pixel, the amount of charge collected by the pixel must be greater than its programmable threshold. Activated pixels send a signal to their ROC containing the pixel's address and a pulse whose height represents the amount of charge that the pixel collected. When a"physics trigger" is generated, each ROC is prompted by its token-bit manager (TBM) to transmit the pixel data, along with additional ROC and TBM information, to the data acquisition system. For every event, the data acquisition system obtains an analog signal containing information on the event number, the ROC address, the last addressed DAC, the address of every hit pixel, and the amount of charge each pixel collected (discussed in Section II, also see Fig. 1) [3].

In the readout process, the signals are transmitted through circuitry that contains programmable voltage supplies, called DACs, that have the ability to tune certain characteristics of the signal. Some of the DAC settings are crucial for obtaining accurate data; for example, one setting may ultimately determine whether or not the data acquisition system receives the correct address of a hit pixel [2, 4]. As a part of the CMS pixel group at Cornell University, I, along with several others, have undertaken the tasks of understanding the effects of these DAC settings, optimizing their values, and developing a DAC-calibration mechanism that will be performed before taking data at the LHC. This calibration will verify that the pixel detector is working properly and help CMS obtain the most accurate data possible.

II. METHODS AND SIGNAL DESCRIPTION

In order to understand and optimize the pixel detector's DAC settings and test our calibration techniques, the CMS pixel group at Cornell University is in the process of constructing a pixel detector test station that will model the apparatus at CERN. The group already has a collection of ROC modules and a TBM that are controlled with a Front End Controller board (FEC), giving us the ability to set DACs and collect data. This is done with a piece of custom computer software, called Cosmo, that communicates with the FEC via USB and with an ADC PCI card in the computer. With Cosmo, DACs can be set and data can be recorded through scripts or a GUI. The ADC card receives data from the TBM just as the data acquisition system will at CERN. Fig. 1, below, shows an example of the ADC data sampled from a TBM connected to a single ROC that has one hit pixel.

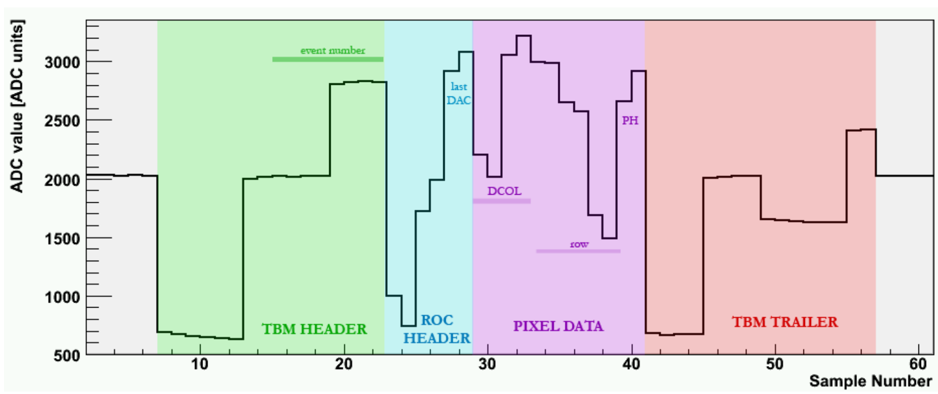

FIG. 1: Analog data signal at doubled length read from a single ROC with one pixel hit sampled at 40MHz. The height of the signal is shown in arbitrary "ADC units". Sections of the signals are distinguished here by different colors, corresponding to different pieces of information that the signal contains (described below).

A single signal read from the TBM contains all of the information about all of the hits that were detected at a single time. Before the data is received by the data acquisition system, or in our case by the ADC, the TBM places all of the information it collects from the ROCs between a *TBM Header*, which contains the number (equivalent to time) of the event and a *TBM Trailer* (green and red, respectively, in Fig. 1). Each ROC read by the TBM precedes any information about hit pixels by a *ROC Header*, which contains the "last DAC" signal that is inversely proportional to the value of the DAC most recently modified (blue in Fig. 1). If there are any pixel hits on a given ROC, its header is followed by information on the address of the hit pixels and the "pulse height", which corresponds to the amount of charge collected by the hit pixel (purple in Fig. 1) [3].

The signal provided by the TBM is analog and therefore has the capability of representing the exact value of continuous information, but almost all of the information contained in the signal is discrete. The address of a hit pixel, for example, is clearly discrete – it is given by two integers, a two digit column address and a three digit row address, corresponding to its coordinates on the ROC. In fact, the only continuous pieces of information in the signal are the "last DAC" and the "pulse height". In order to represent a piece of discrete information, the analog signal makes transitions between discrete voltage levels. At a given time, the signal will to take on one of up to six values (from lowest to highest ADC value: *ultrablack, 0, 1* a.k.a *black, 2,3,4,5*), giving it the ability to represent a base six number. With events at the LHC happening at a rate of 40MHz, it is essential that data readout is fast, thus the signal transitions between levels every 25ns [1, 3].

III. CALIBRATIONS

A. Address Level Calibration

In order to accurately transmit and decode the discrete information in the analog signal, it is necessary that the values that the analog signal take on are near the intended levels and completely distinguished from the other levels. At Cornell, we have focused on distinguishing the pixel addresses. Fig. 2, below, is a histogram of the values taken on by one of the signal's address locations after achieving address distinction.

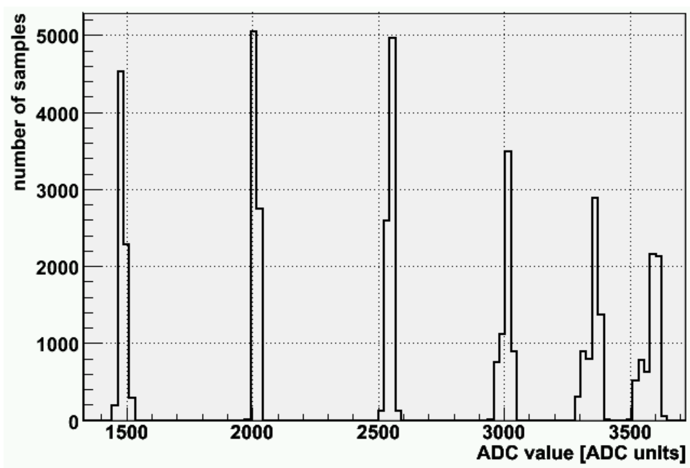

FIG. 2: ADC value histogram showing distinguishable address levels

Designing apparatus that is capable of transitioning between distinct levels in just nanoseconds has proven itself difficult – due to a slight excesses in capacitance in our TBM, the signal does not always reach its intended level in time to be sampled correctly, especially when making a transition between the more distant levels. This has been corrected in newer TBMs, but with an older version, we have been forced to modify our data taking techniques to achieve level distinction. Rather than only sampling once per 25ns clock cycle, we have doubled the signal length while continuing to sample at the same frequency. This gives us two samples per clock cycle, and by using only the second, we give the signal more time to reach its intended values. In addition, exactly where the sample takes place within the second part of the clock cycle was optimized by adjusting the delay (relative cable lengths) between the ADC's external trigger and the TBM's signal to 10ns.

Even with these changes, levels *4* and *5* were indistinguishable when using the default DAC settings. We found that the DAC *VIbias_roc*, had a significant effect on the separation of address levels. The value of *VIbias_roc* was optimized by looking at the address level distinction as its value was varied through its range. As seen in Fig. 3 below, the address levels, including those of *4* and *5*, are distinguishable at a value of *VIbias_roc = 110*.

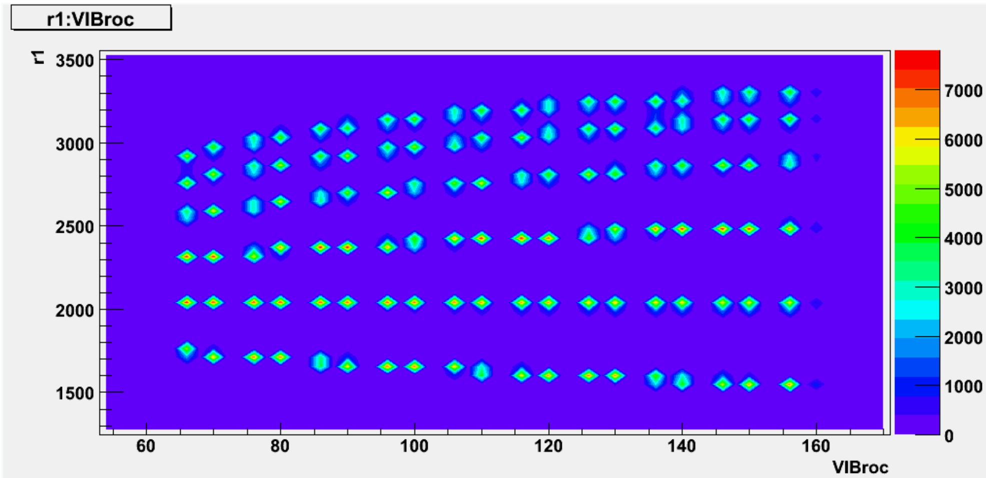

FIG. 3: Number of hits at each possible ADC value as *VIbias_roc* is varied

B. Gain Calibration and Optimization

The pulse height is received by the data acquisition in arbitrary ADC units that can be related to the amount of charge collected by a given pixel by a "gain calibration" [2, 4]. To obtain a gain calibration, or "gain curve", pixel hits are generated by injecting known amounts charge with the *Vcal* DAC and measuring the resulting pulse height. The gain calibration can saturates at higher *Vcal* values due to limitations in the ROC electronics. This saturation should be minimized so that the pixel detector is sensitive to the largest range of charge possible. One way to quantify the length of this range is by finding the Linear Range of the gain calibration, which is arbitrarily defined as length of a line (light blue in Fig. 4) – whose equation is found by fitting the gain curve for 30 *Vcal* units after the first 5 (red in Fig. 4) – between 5 *Vcal* units after the beginning of the fit and the *Vcal* value at which the fit differs from the data by more than 100 ADC units (dark blue in Fig. 4) [6].

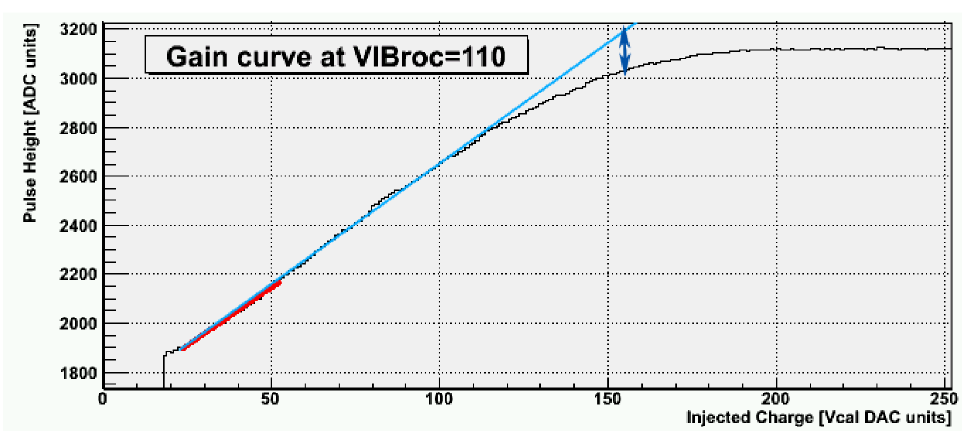

FIG. 4: Gain Curve showing the definition of the Linear Range

The largest part of our work in optimizing the Linear Range was to reproduce the results presented by Sarah Dambach of the Swiss Federal Institute of Technology in Zürich. This allowed us to both verify her results and develop our own the analysis code at Cornell. As presented by Dambach, two DACs known as *VOffsetOp* and *VoffsetRO* are the most relevant to the Linear Range [6]. To optimize the Linear Range with respect to these DACs, the Linear Range was measured as *VOffsetOp* and *VoffsetRO* were varied through the ranges of their possible values. The results are shown below in Fig. 5, where the left plot shows the Linear Range as a function of the DACs and the right plot is a linear fit of the means from a Gaussian fit of Y-slices of data. This line gives the optimal values of *VOffsetOp* and *VoffsetRO*.

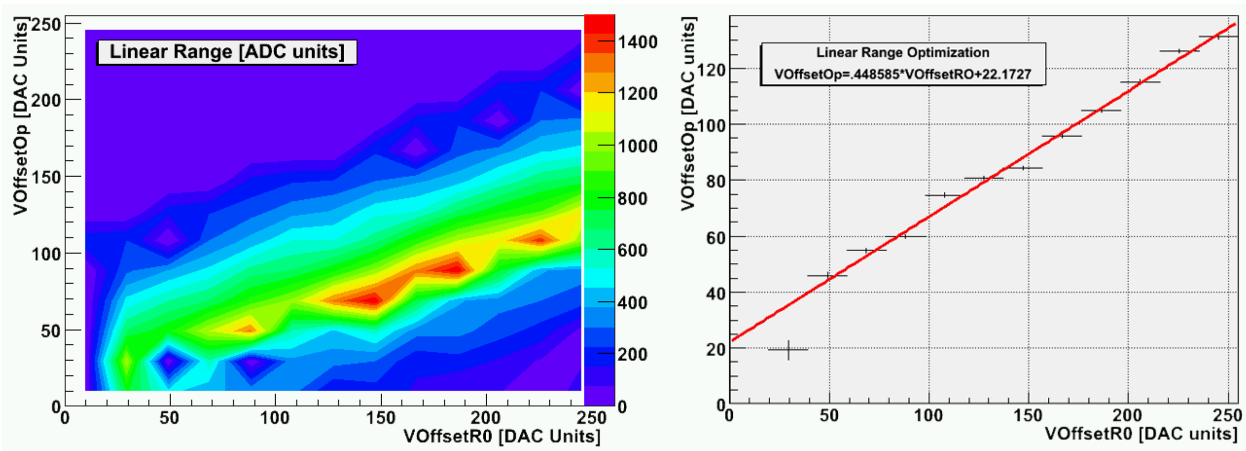

FIG. 5: Linear Range optimization of *VOffsetRO* (R) and *VOffsetOp* (P)

Because *VIbias_roc* was changed from its default value in order to distinguish address levels 4 and 5, its effect on the linear range was studied to ensure that the Linear Range was not being negatively affected. We found that at low values of *VIbias_roc*, the Linear Range significantly decreases, so a value below ∼100 should not be used.

C. Threshold Calibration

Due to variations in the ROCs and the pixels, the effective thresholds of the pixels can vary significantly. To correct the effects of these variations and achieve the same sensitivity to ionization for every pixel, each pixel is given a digital *trimbit* setting between 0 and 15 that changes its effective threshold, and each ROC is equipped with two DACs designed to change the effective threshold of every pixel on the chip – one, called *VthrComp* or *VcThr*, that adds a constant, and another, called *Vtrim*, that that determines the range of the *trimbit*'s correction [2, 4]. The effects of each of these settings was studied, and some of the results that show the general behavior of each are shown below in Fig. 6 and Fig. 7.

As suggested by our data, the effective threshold is related to the settings by

$$Threshold_{effective} = -C_o VcThr - C_1 Vtrim \frac{15 - trimbits}{15} + C_2 \qquad (1)$$

where C_n are positive calibration constants [8, 9]. Depending on the accuracy required, non-linear fits that would change Eq. 1 could be used. We are currently working on writing an algorithm that can be used to optimize these three settings to obtain the narrowest effective threshold distribution possible before taking data [4, 7].

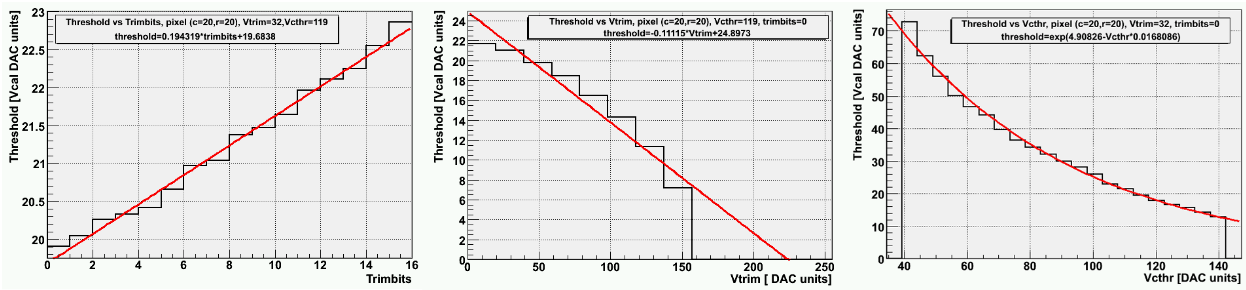

FIG. 6: The effects of the *trimbits*, *Vtrim*, and *VcThr* on the effective threshold

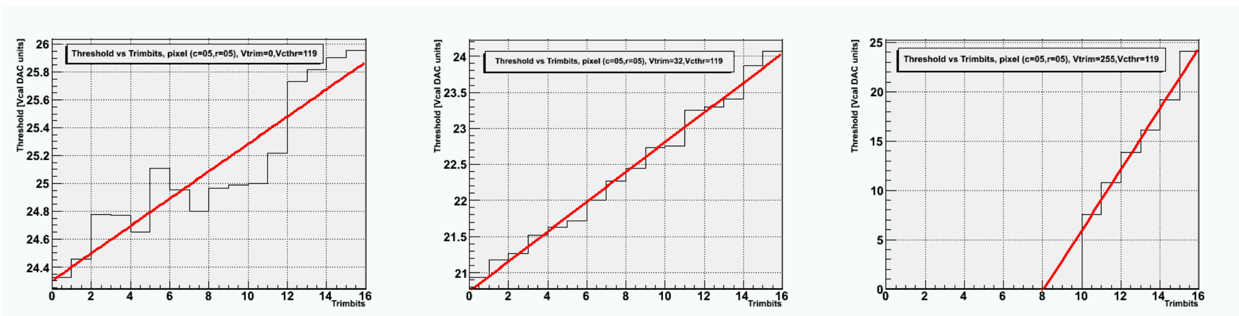

FIG. 7: The effect of *Vtrim* on the strength of the *trimbit* correction

IV. TEST STATION IMPROVEMENTS

The CMS pixel group at Cornell is preparing to make a significant addition to the existing test station that will allow us to model the entire pixel detection and data acquisition system that will be used at the LHC. Most recently, a VME crate and a CAEN computer to VME controller optical link were set up and tested by writing and reading to memory. Additional improvements included setting up a second test station computer, upgrading our TBM, and modifying our ADC external trigger signal with NIM to avoid missing data.

V. CONCLUSIONS

By doubling the length of the output signal, adjusting the relevant cable lengths, and adjusting *VIbias_roc*, we are now able to achieve address level distinction, allowing us to accurately determine the address of hit pixels. Gain calibrations and Linear Range measurements were performed through the ranges of *VOffset_Op* and *VOffset_RO*, the most relevant DACs to the length of the Linear Range. Their values were optimized, giving us sensitivity to the largest range of collected charge possible. The effects of the pixel trimbits and DACs *VcThr* and *Vtrim* on the detector's effective threshold were studied in order to begin developing a threshold trimming algorithm that will give all pixels the same sensitivity to charge.

The next step in this work will be to modify the existing data acquisition scripts and optimization algorithms to process calibration data more similar to what the detector will need to collect at the LHC – calibrations will have to be performed quickly and for many pixels at a time in order to be completed in a reasonable amount of time. The CMS pixel group at Cornell is already on their way to accomplishing this goal. LHC-style calibration data has already been taken and the optimization algorithms are currently being developed. In addition, as we continue to understand the effects of other DACs, their values can be optimized in order to obtain the most accurate data possible at the LHC.

VI. ACKNOWLEDGMENTS

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