Pixel Detector For ATLAS Phase-2 Upgrade: Tracking In Very Forward Rapidity Region

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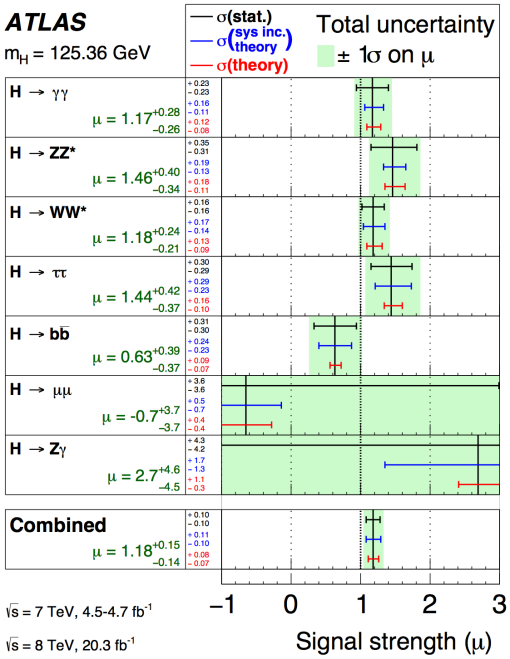
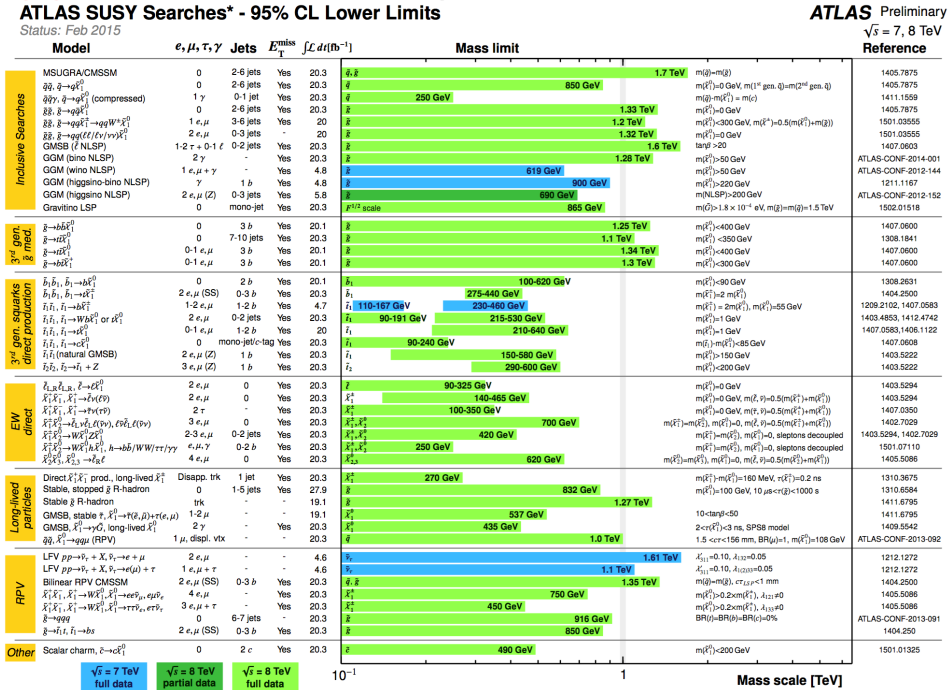
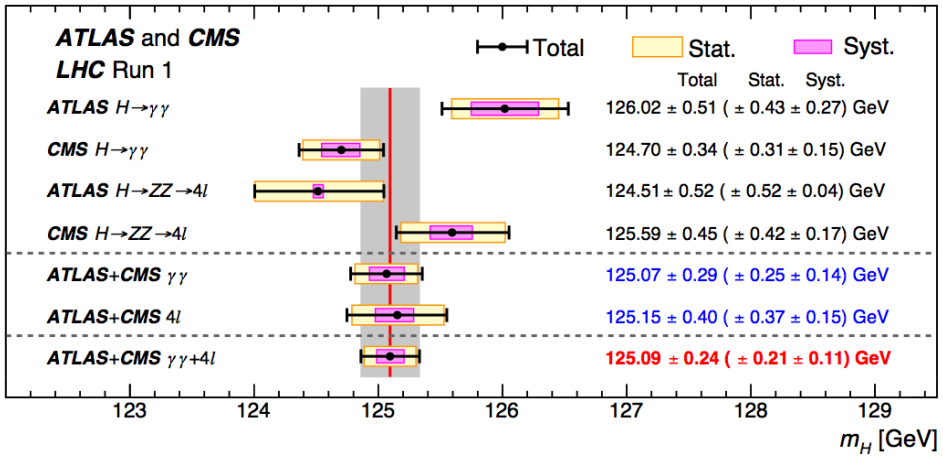
(LBNL)

Higgs Boson Discovery: Triumph Of LHC Run-1 Program

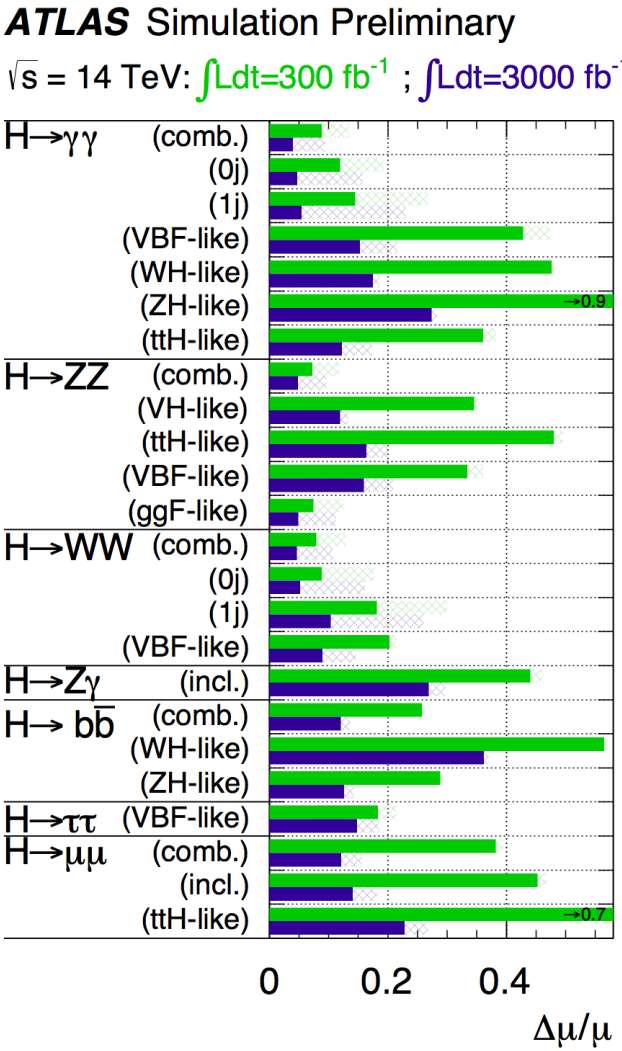
Main Run-1 results: discovery of Higgs boson; no signs of New Physics



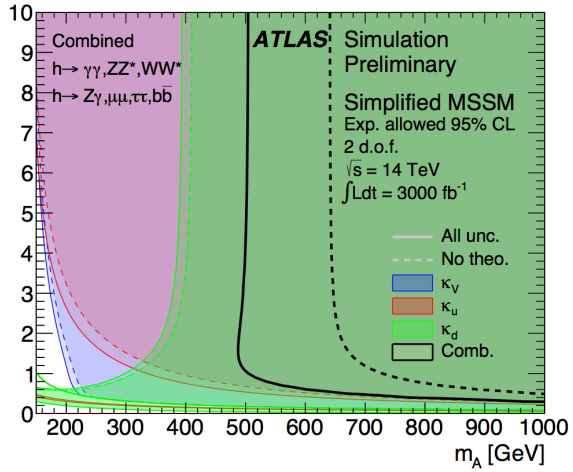


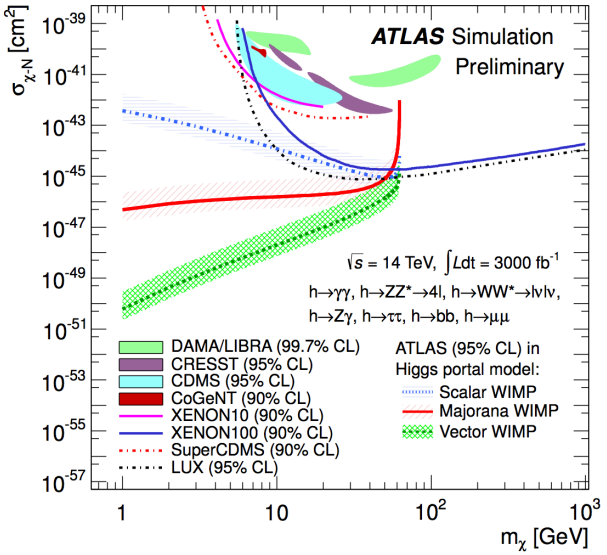


Physics Program For High Luminosity LHC

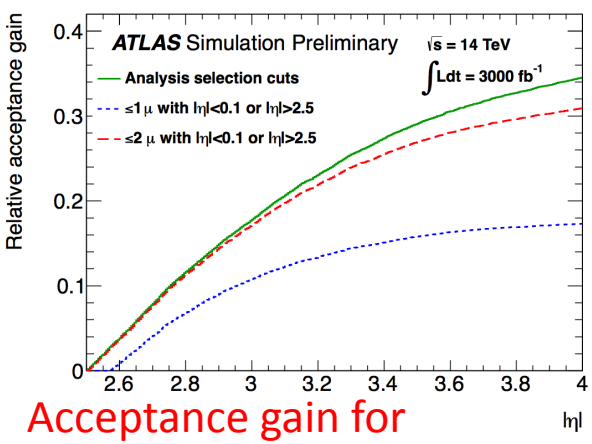


- Precision measurements of Higgs boson production and decay rates
- Observation of rare Higgs boson decays
- Search for HH production
- Search for new physics

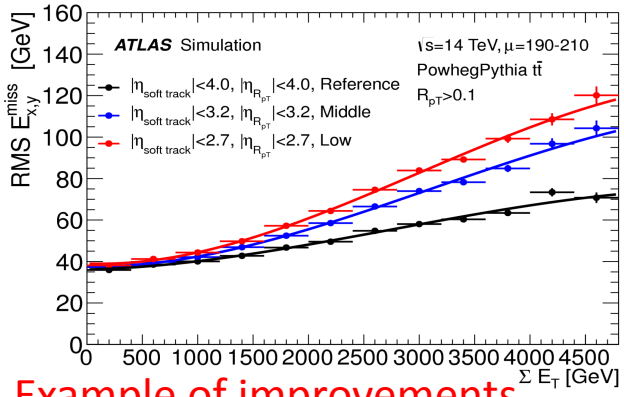




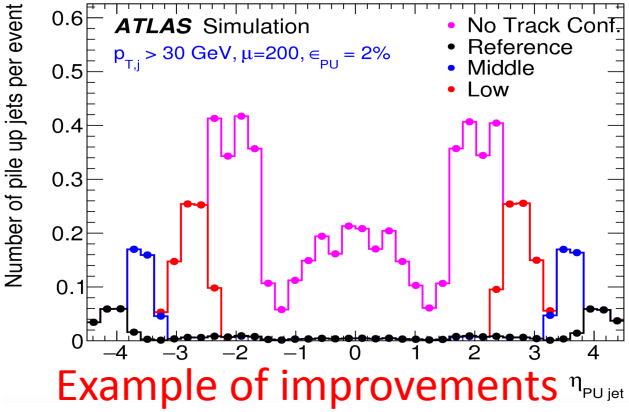
Tracking Is Crucial For Success Of HL-LHC Program



Acceptance gain for $H \rightarrow ZZ^* \rightarrow 4\mu$ decays



Example of improvements in MET resolution



Example of improvements in pile-up jet rejection

- ATLAS tracking detector during HL-LHC run will have to provide efficient and precise track reconstruction in a very challenging environment with ~200 pile-up interactions per bunch crossing
- New detector must cope with high radiation field (up to 7.7 MGy and $1.4 \times 10^{16} n_{eq}$ cm^{-2})
- **All silicon tracking detector: pixel detector + strip detector**
- Extension of the tracking coverage into the very forward region (up to $|\eta| < 4$) will significantly enhance the potential of the HL-LHC physics program

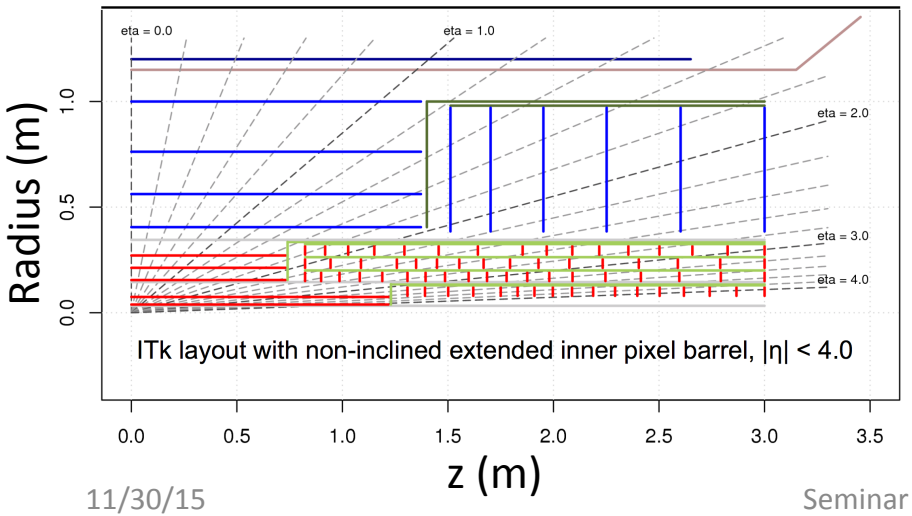
Extensive R&D Program Is Well Underway

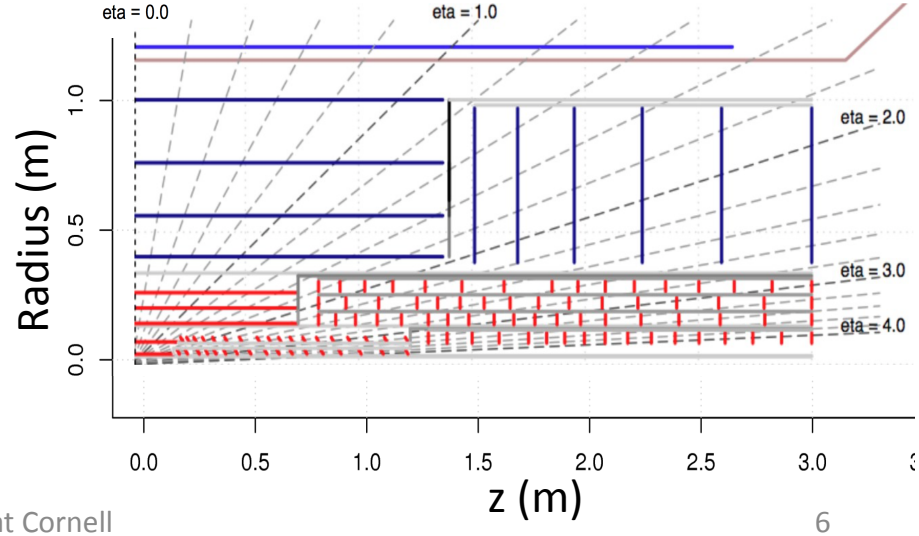
- Technical Design Report (TDR) for Strip detector is due in 2016
- TDR for Pixel detector is due in Q4 of 2017
  - Pixel sensors (planar, 3D, CMOS,…)
  - New FE chip (RD53)
  - Module design, module electronics
  - Services
  - Local supports
  - Off-detector electronics
  - Global mechanics
  - Layout optimization
  - Software development

} This seminar

Two Concepts Of Pixel Detector For Phase-2 Upgrade

- Tracking in the forward region (|η|>2.7) will rely solely on Pixel detector
- Two concepts of the Pixel detector are under study
  - Concept-1 ("Extended") utilizes long clusters from extended inner barrel layers
  - Concept-2 ("Inclined") utilizes inclined modules in two inner barrel layers
- Two layouts under study have the same Pixel end-cap
- Both layouts are optimized to have at least 9 space points for all η
- Choose final layout based on the comparison of performance (March 2016)
- Further optimize the chosen layout to achieve most optimal performance



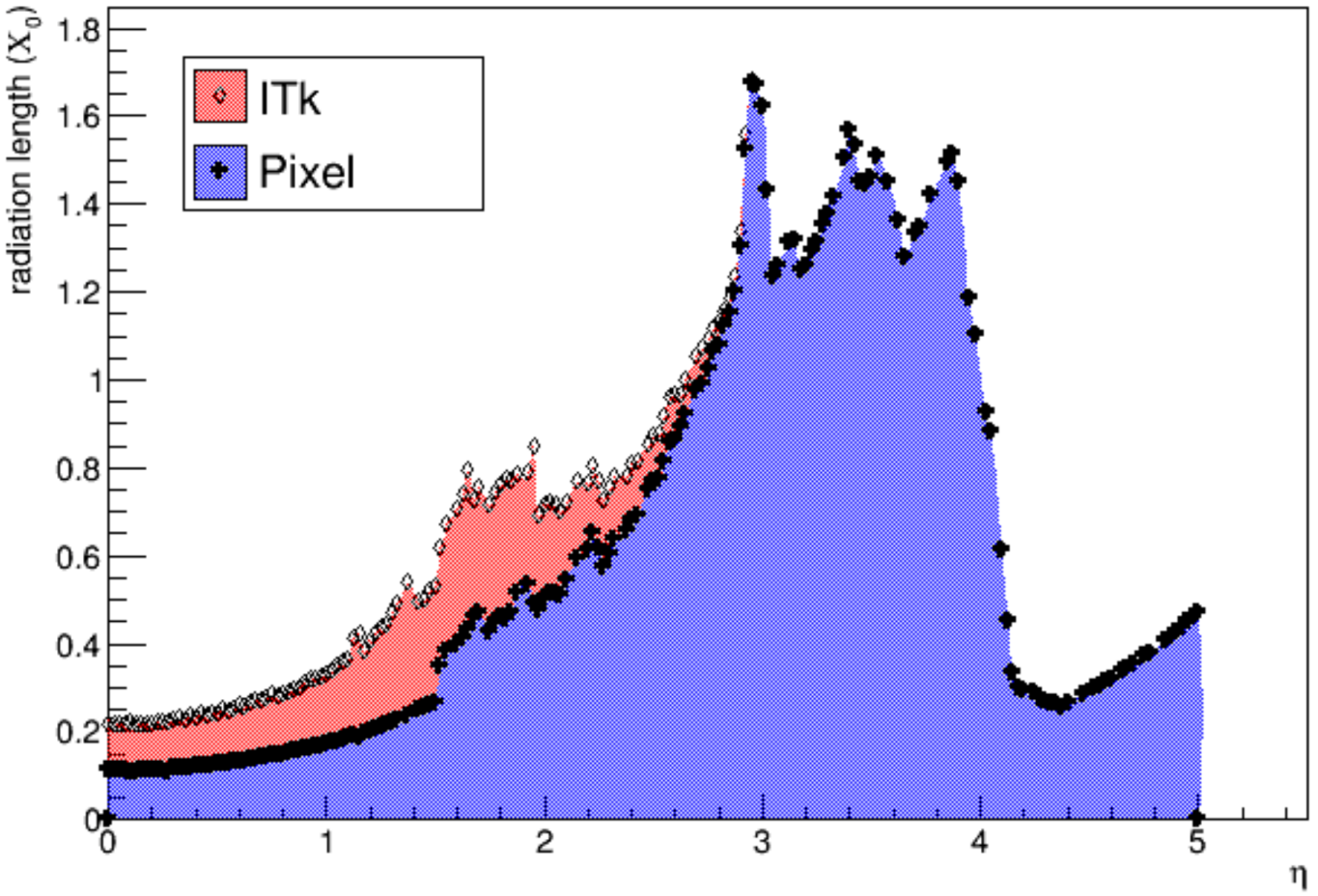


Pixel Detector For Phase-2 Upgrade

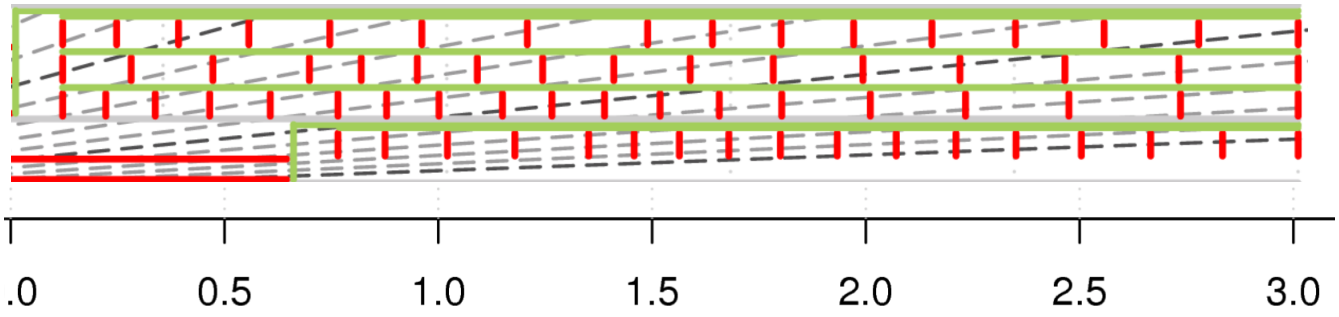
- Sensors
  - Planar sensors n-in-p (for now, R&D is ongoing)
  - Barrel Layer-0,1 and inner end-cap ring: 50μm × 50μm × 100μm
    - Also consider option of 25μm × 100μm × 100μm
  - Barrel Layer-2,3,4 & end-cap: 50μm × 50μm × 150μm
  - Aim at operating with 600e threshold(s)
  - Electronics noise hit occupancy: 10^{-6}
- Modules: "quad" modules everywhere (except for Layer-0, "double")
  - About 10,000 modules
- Barrel: 5 layers
  - R=3.9, 6.5, 16, 20, 30 cm
  - room for 6^{th} layer, study of potential benefits are underway
- End-cap: 4 layers of rings, number of rings vary depending in η and R
  - R=15-19, 21-25, 27.5-31.5, 33.5-37.5 cm
- Total surface is ~14 m^2
  - depends on layout, roughly 50/50 between barrel and end-cap
  - approximate cost is 38.5MCHF

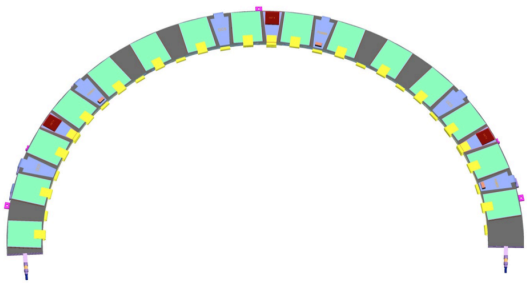
Amount Of Material For Phase-2 ITK Detector

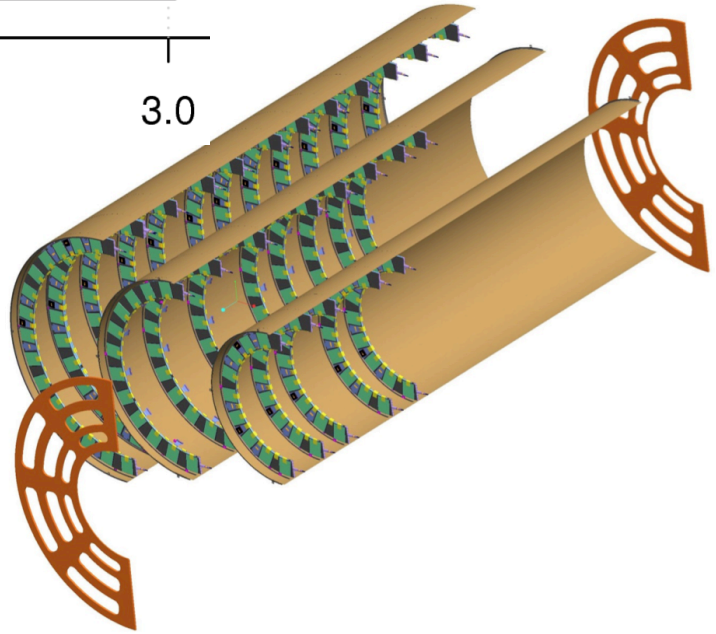
- Preliminary estimates for the "Extended" layout
  - This will change with more refined knowledge of services and after layout is finalized



End-cap Pixel Detector

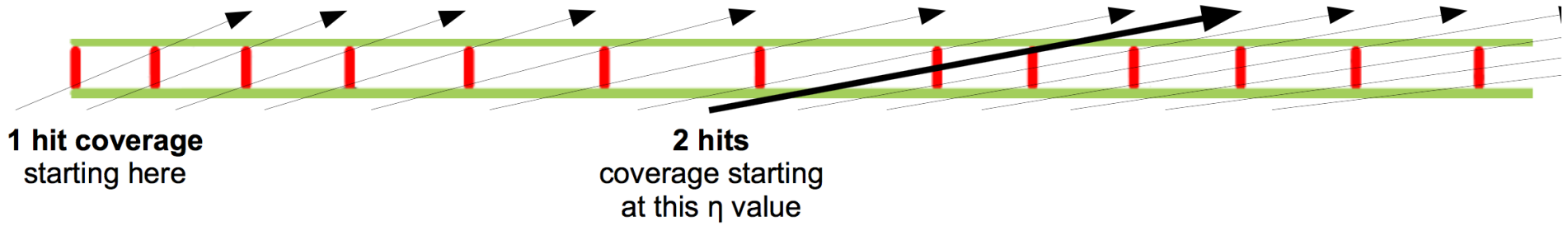






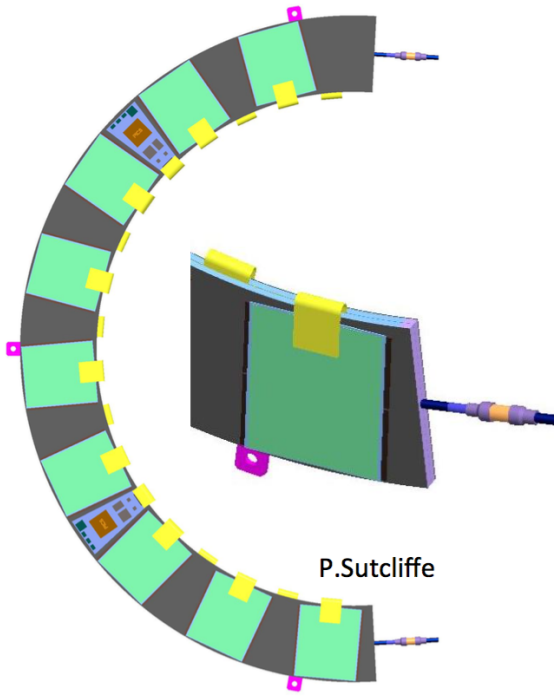
- Highlights of design
  - Highly flexible design: individual rings can be placed where they are needed
  - Services can be routed in between rings: greatly simplifies the build
  - Use 4-chip “quad” modules: common development with barrel staves
  - Highly modular design: same elements everywhere, just scale is different
  - Intergration into ITK can be “monolithic” (in one piece) or “modular” (in sections)

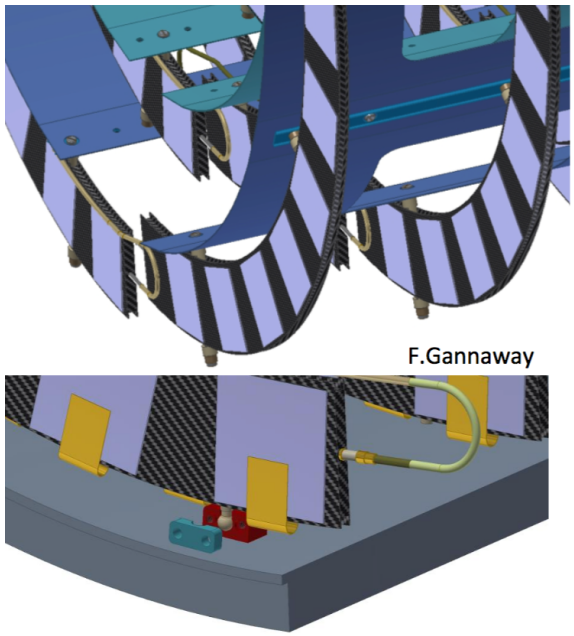
Ring Position Optimization For End-Cap



- For a given η range, each ring layer contributes a given number of hits
  - Allowing for some overlap between consecutive modules
  - Respecting a minimum distance of 8 cm between rings
- A similar principle is used for positioning the inclined barrel sensors

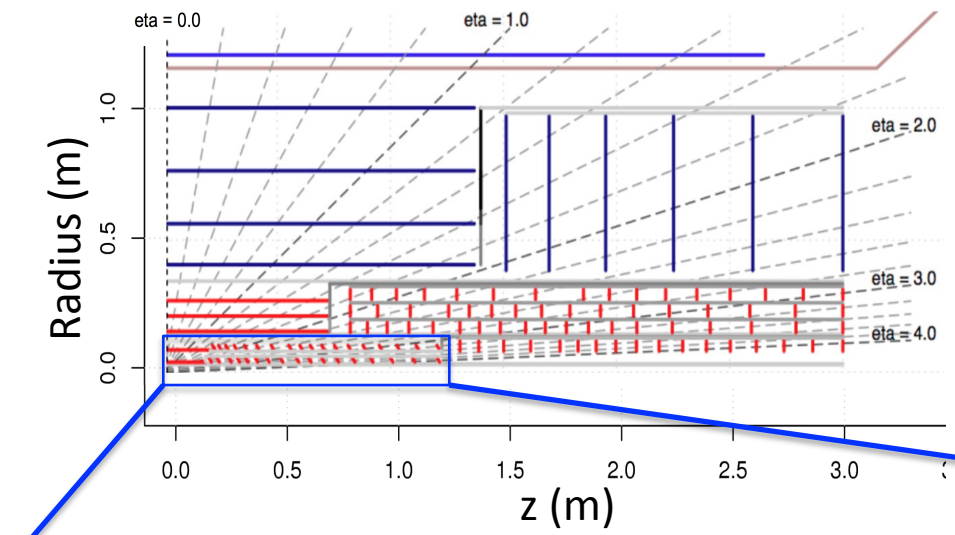
Ring Design For End-Cap

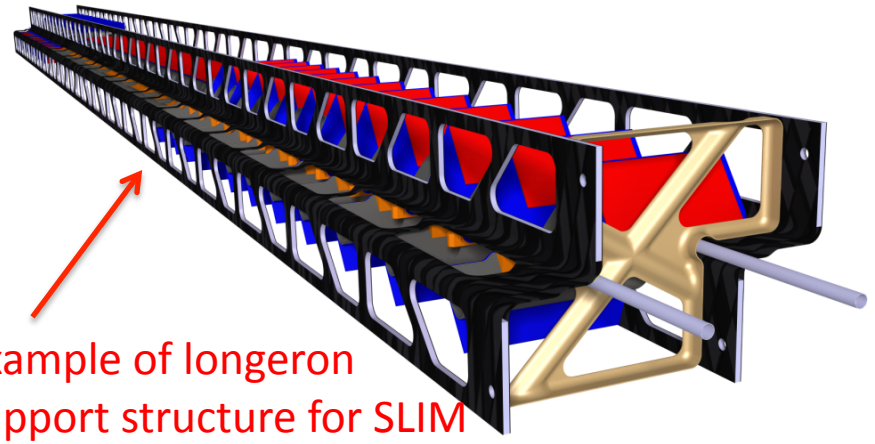




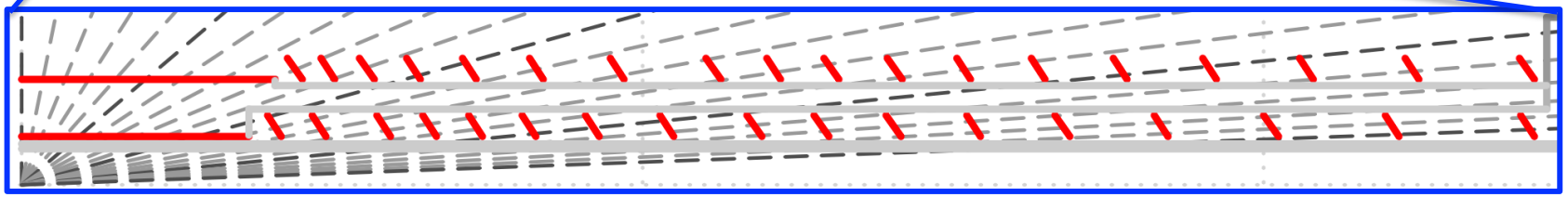
- Mechanical design is quite mature
  - Carbon fibre/foam sandwich
  - Embedded bus tape and cooling pipe
  - "Eos" card on surface for power and DCS
  - Currently assuming no GBTx–twinax routed directly from modules
- Each ring layer is attached to a support cylinder at the outer edge

“Inclined” Layout For Pixel Barrel Detector



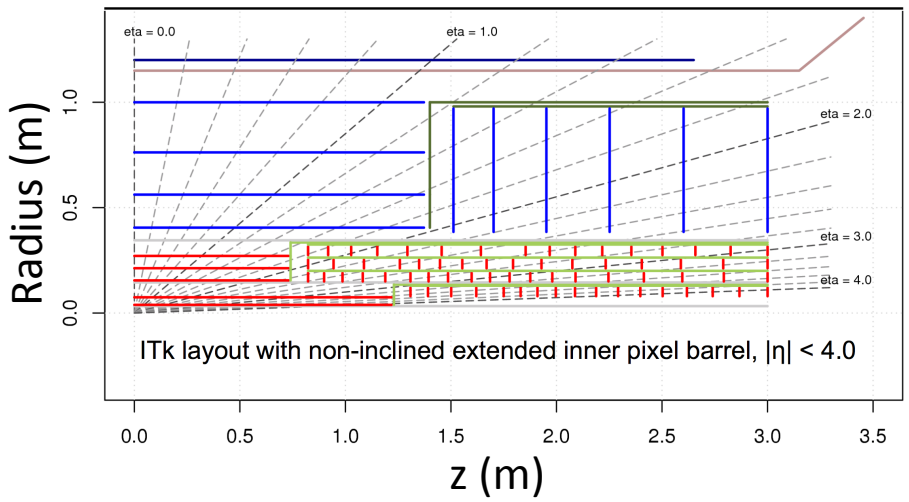


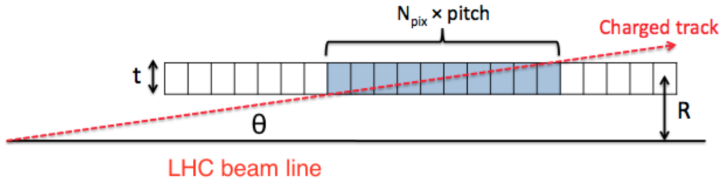
Example of longeron support structure for SLIM



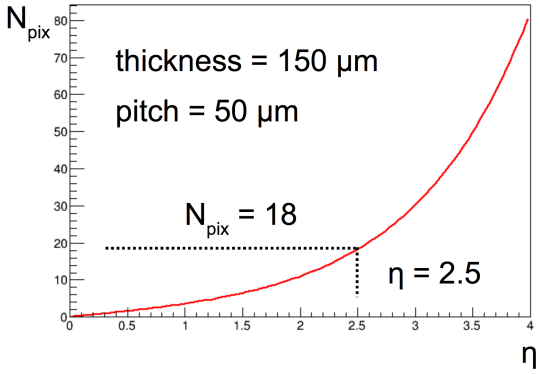
- Modules inclined at 34° with respect to vertical line
- Helps to reduce amount of material traversed by a track
  - Reduces effect of multiple scattering and silicon area
- Provides (≥1 for given η) hits very close to interaction point
- Two technologies: “Alpine” and SLIM

“Extended” Layout For Pixel Barrel Detector

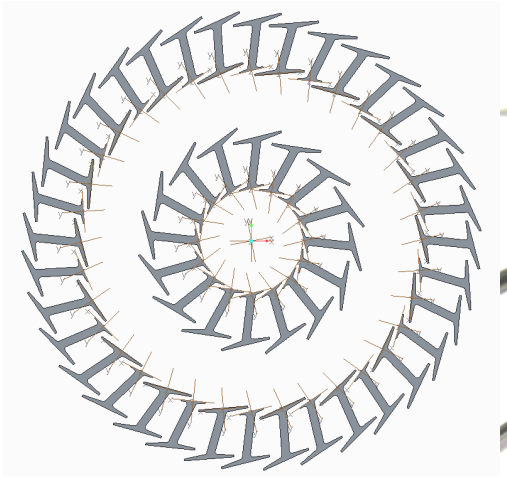


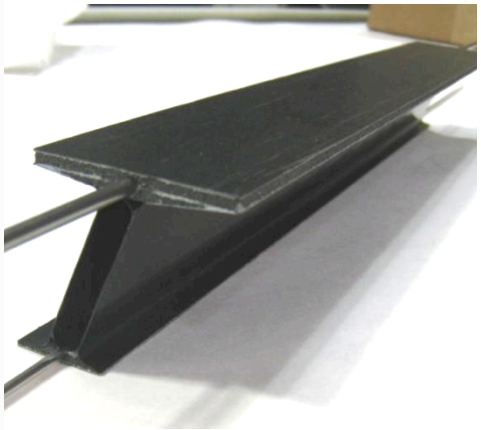


$$\tan\theta = \frac{t}{N_{pix} \times p}$$



I-beams: low-mass carbon composite support structure





- Long clusters = “tracklets”, providing initial precise estimates of θ and z_0
  - Seed pattern recognition
  - Potential to reduce fake rate
  - Potential to reduce CPU time
- Simple and easy to build design

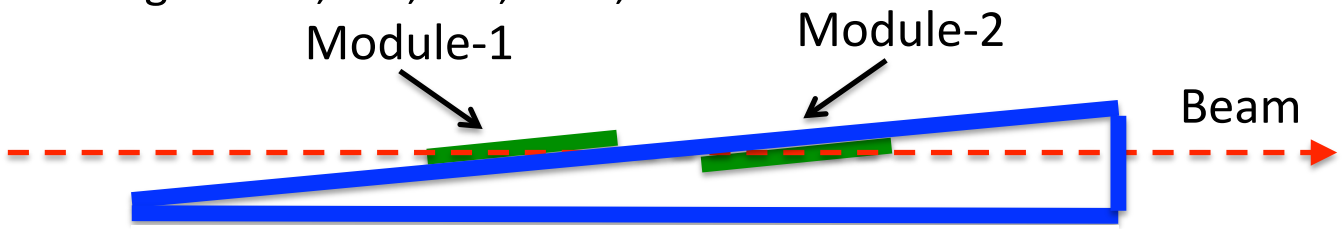
R&D Program For "Extended" Pixel Barrel Detector

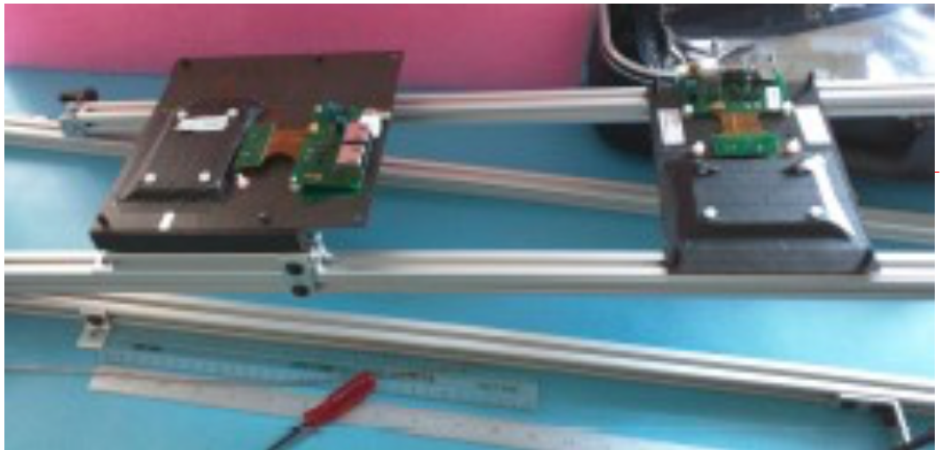
- Institutions involved: **LBNL**, U. Louisville, U. Wisconsin

- Test beam to study clusters at very small incidence angles (this talk)
- Comparison of simulation with test beam results
- Development of pattern recognition based on cluster size (this talk)
- Tests of pattern recognition based on cluster size with simulation (this talk)
- Optimization of the layout
- Study of tracking performance and benefits to physics program with the optimized layout
- Test beam studies of the proto-type detector at very small incidence angles

SLAC ESA Test Beam

- Four un-irradiated Insertable B-Layer (IBL) modules
  - Two double-chip planar modules; two single-chip 3D modules
  - Most modules have FEI4B chips (one module with FEI4A chip)
  - Planar sensors: 50µm × 250µm × 200µm
  - 3D sensors: 50µm × 250µm × 230µm
  - Modules tuned to 10 ToT at 16K electrons
- Beam: 10 GeV electrons, a few particles per bunch at 5 Hz
  - Studies with beam in "short" (50 µm) and "long" (250 µm) directions
  - 5 incidence angles: ~2°, ~4°, ~6°, ~10°, ~15°





CERN SPS Test Beam

- Single-chip 3D module with FEI4A chip
  - 5 incidence angles: ~2°, ~4°, ~6°, ~10°, ~15°
- Beam: charged pions (π^+) with 180 GeV
- Tracks measured with FEI4 telescope with 14µm and 8.5µm resolution in *X* and *Y*

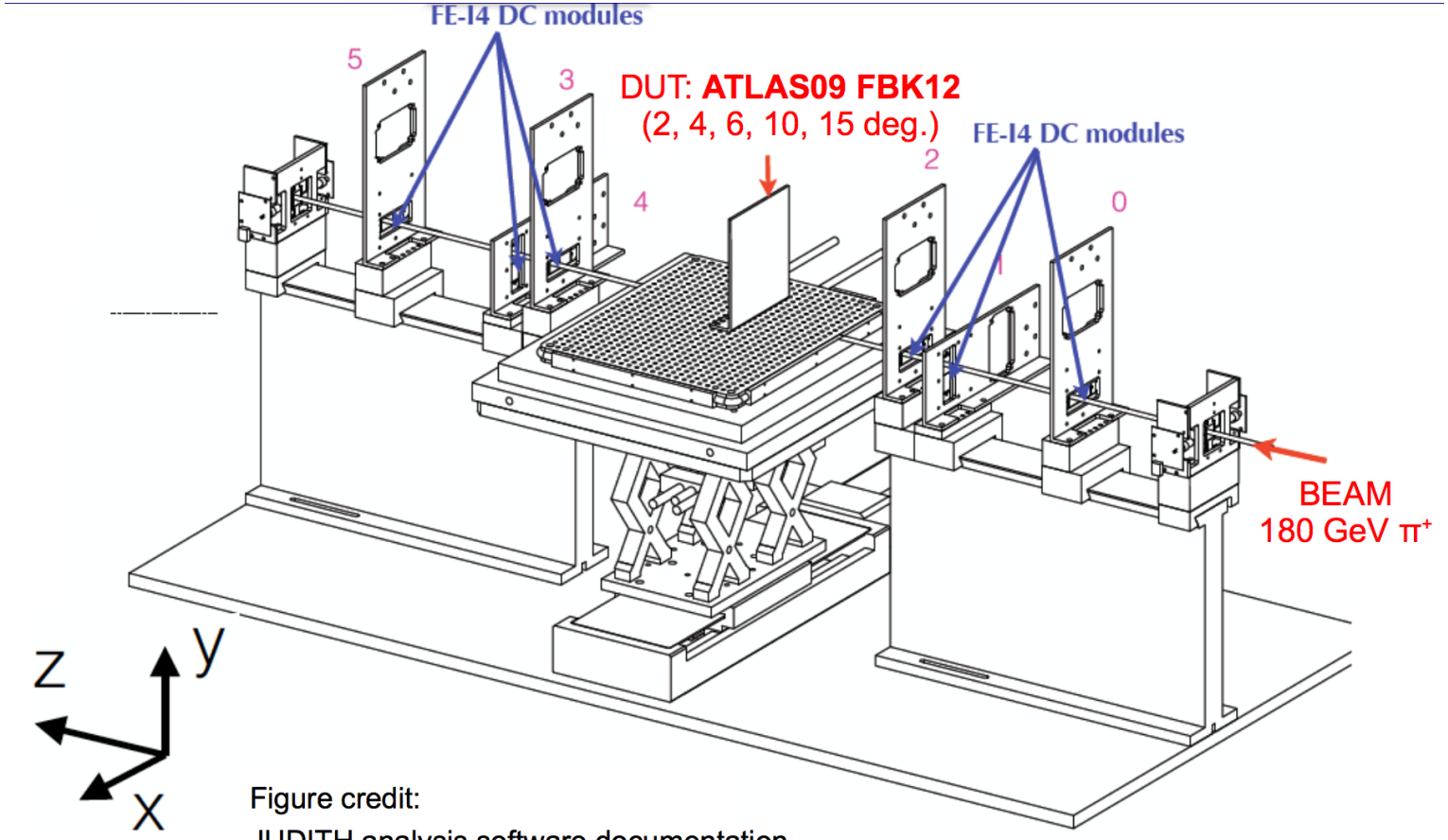
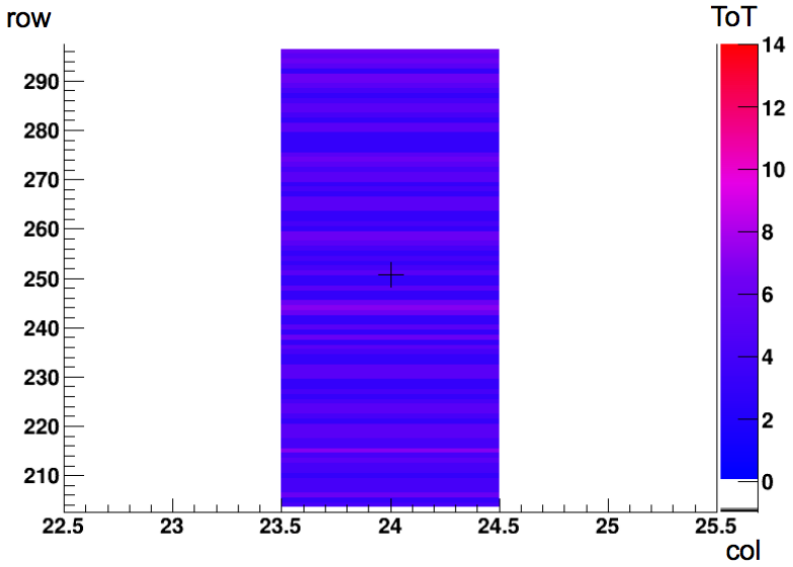
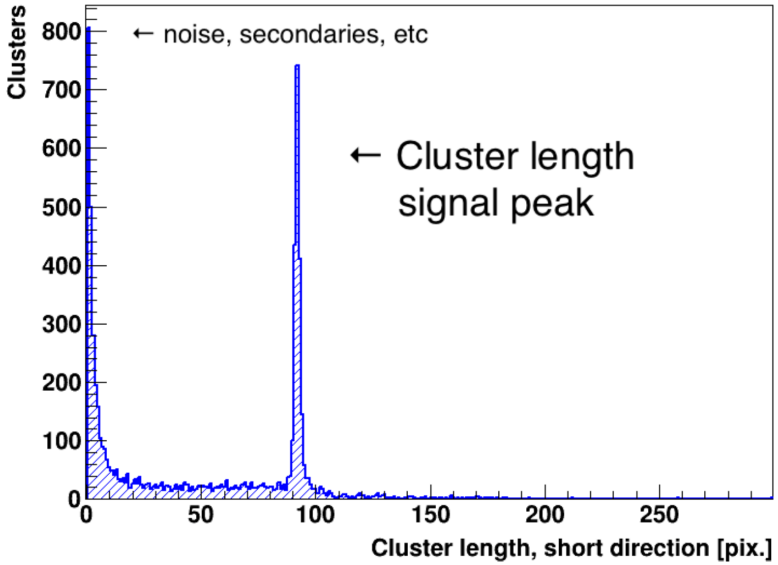


Figure credit:
JUDITH analysis software documentation

Long Pixel Clusters Observed



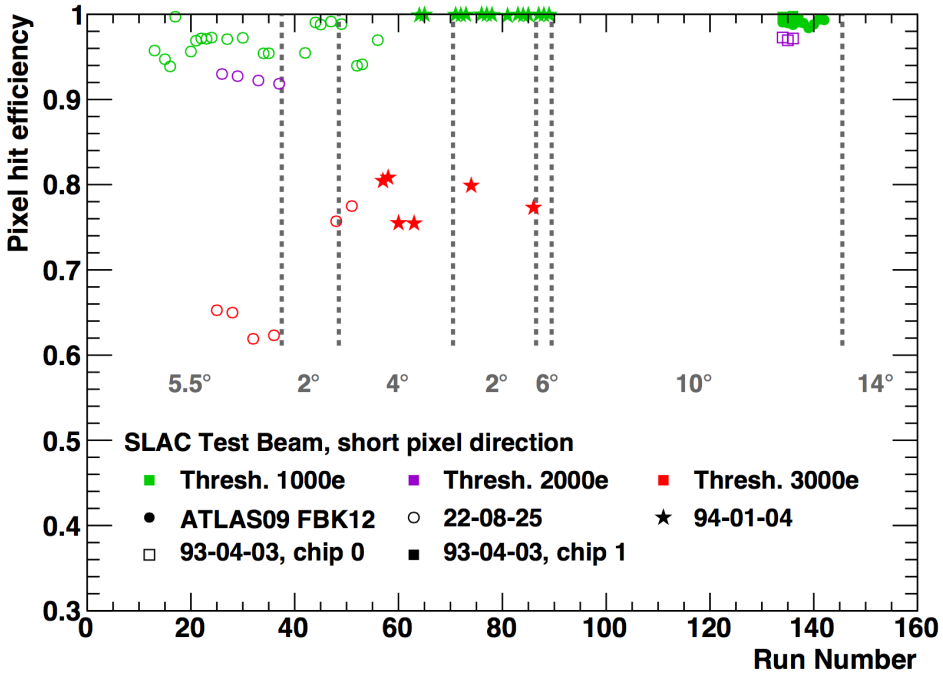


- Example of typical clusters at ~2.5° (η~3.8)
- Planar module biased at -180V and with 1000e threshold
- Beam is in "short" (50μm) direction
- "On-peak" cluster size is 93 pixels

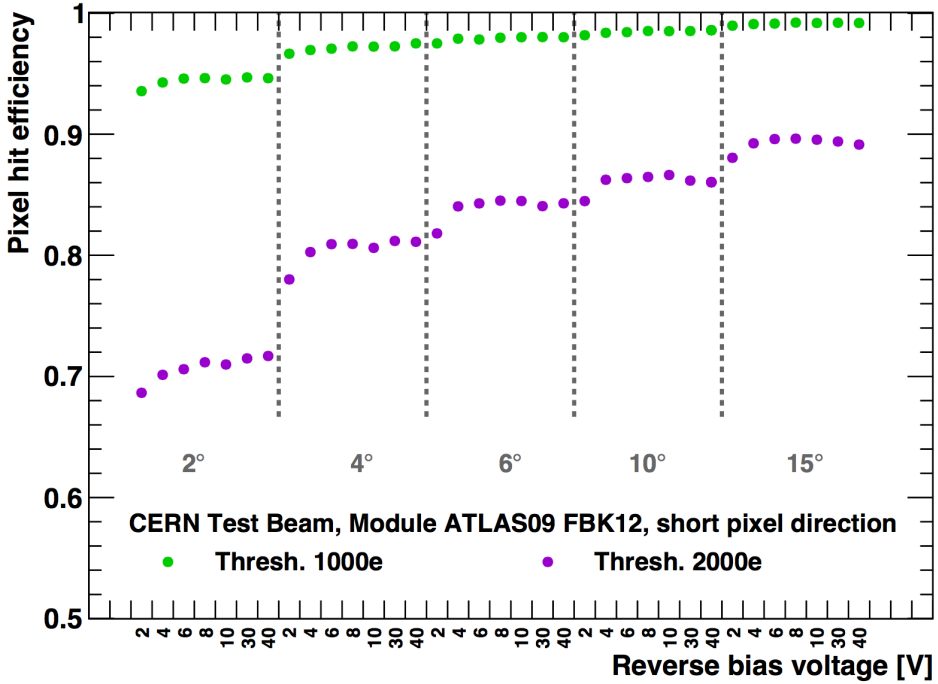
Pixel Hit Efficiency In Test Beam Data

- Efficiency for "long" direction is >99.5% for all modules at all angles, thresholds and reverse bias voltages
- Efficiency for "short" direction has strong dependence on threshold
  - Efficiency in 3D modules also shows some dependence on incidence angle and reverse bias voltage

No timing cut applied



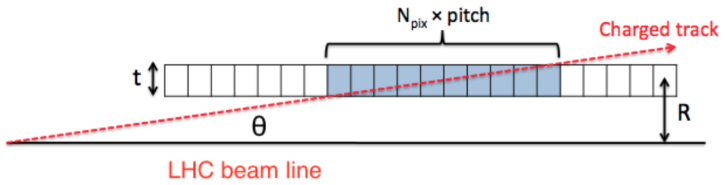
Example: ε = 4/5 for this long cluster



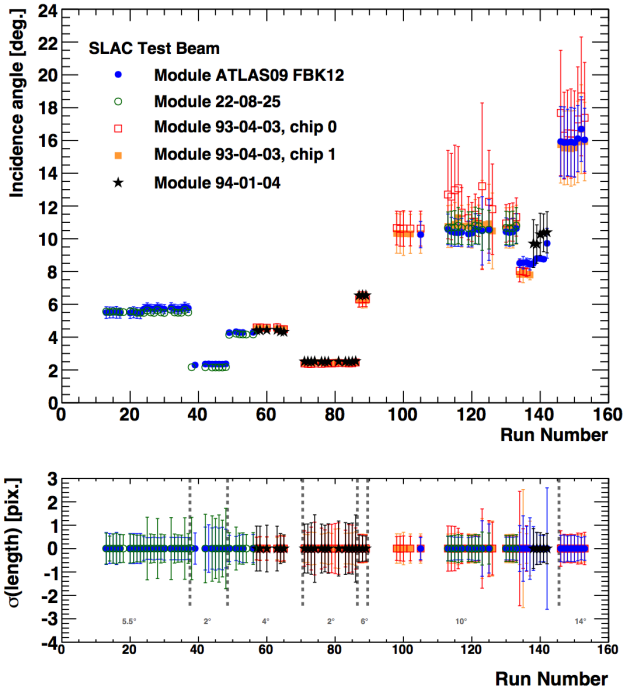
Cluster Length And Measurements Of Incidence Angle

- Cluster length provides precise measurement of incidence angle
  - Results are essentially independent of the threshold
- Consistent results between "short" and "long" directions in SLAC and CERN data
  - ~2% resolution is achieved for tanθ at θ~2° for "short" direction

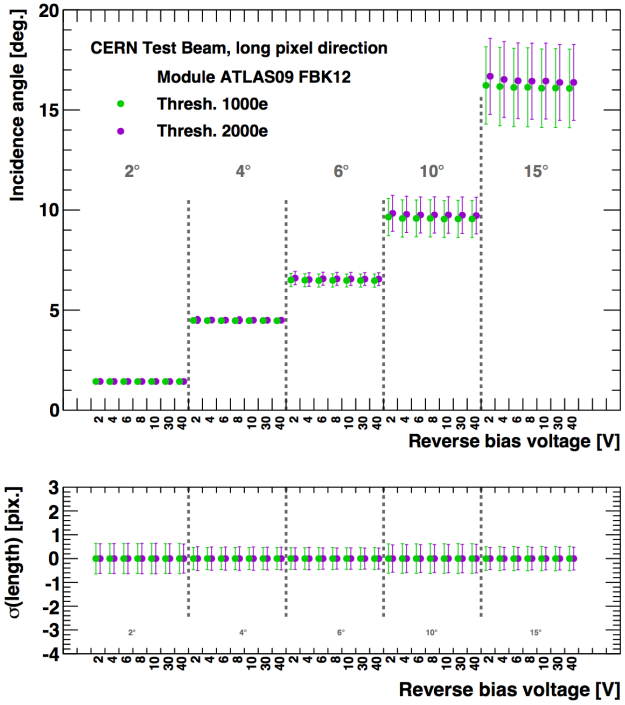
$$\tan\theta = \frac{t}{\left(N_{pix} - \delta\right) \times p}, \quad \delta = 1$$



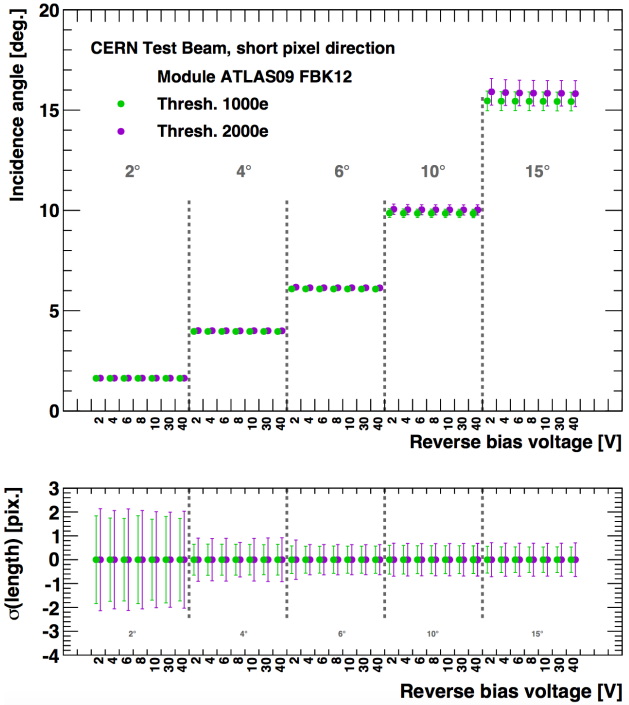
SLAC data



CERN data: 250µm direction

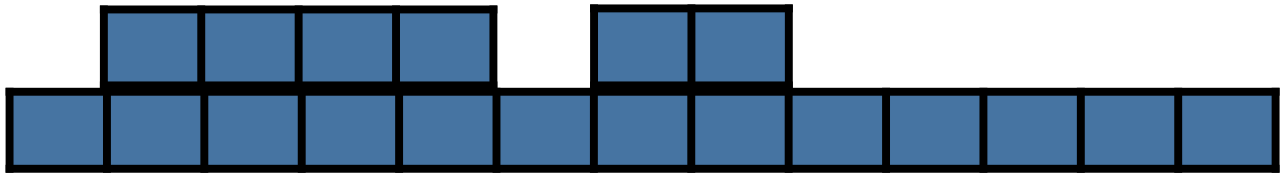


CERN data: 50µm direction



Measurements Of Charge Sharing And Charge Collection

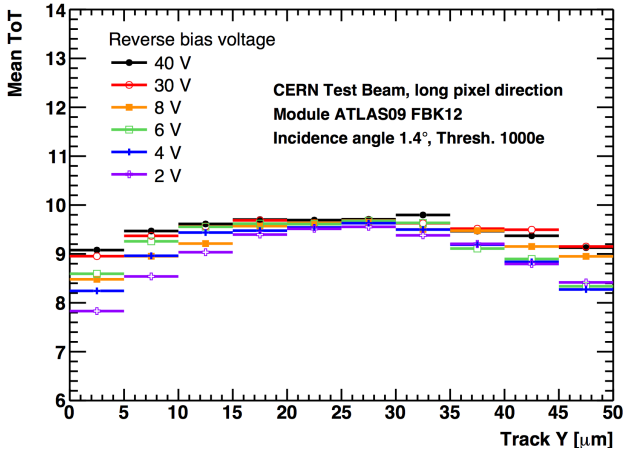
- Measurements performed using CERN data for 3D module as a function of reversed bias voltage
- Charge collection is smaller closer to pixel edges, effect is more pronounced at smaller bias voltages
- Charge sharing is larger at pixel edges and lower bias voltage



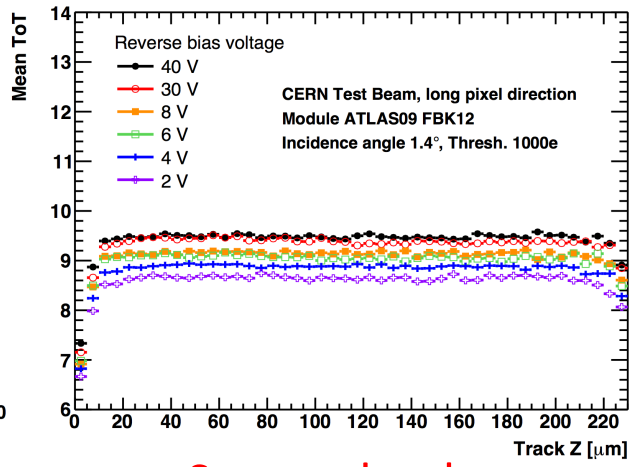
N_m: number of pixels in main row

N_n: number of pixels in neighboring row

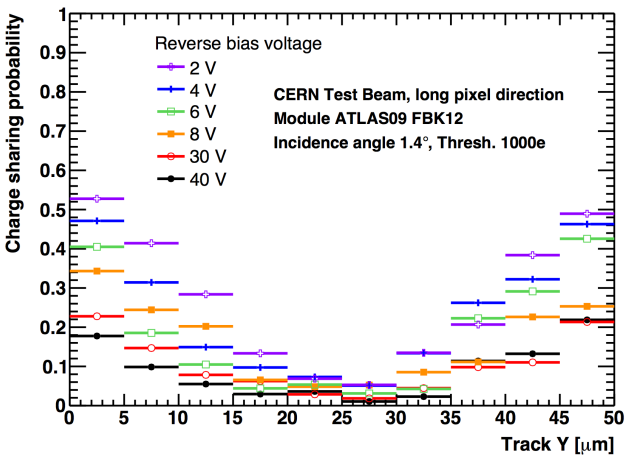
$$P_{sh} = 1 - \frac{N_m - N_n}{N_m + N_n}$$



Direction perpendicular to beam



Sensor depth

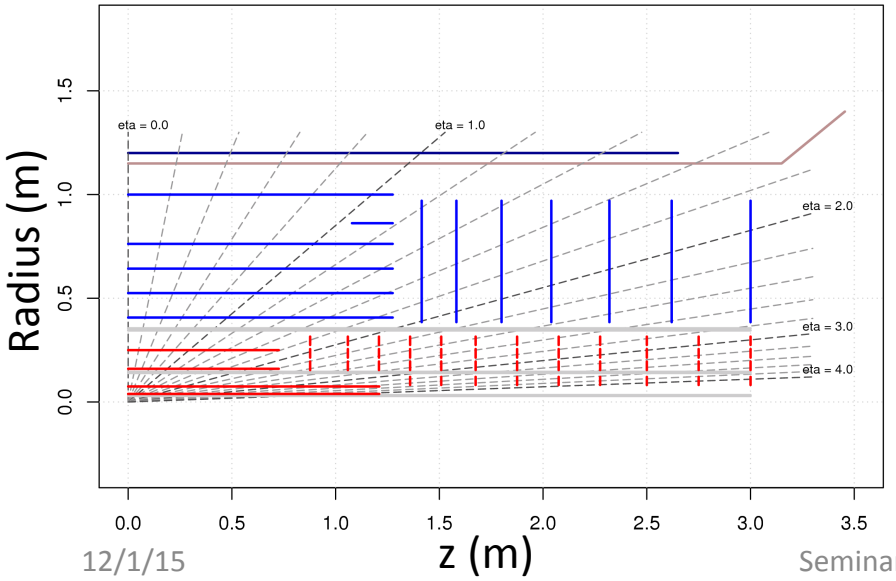


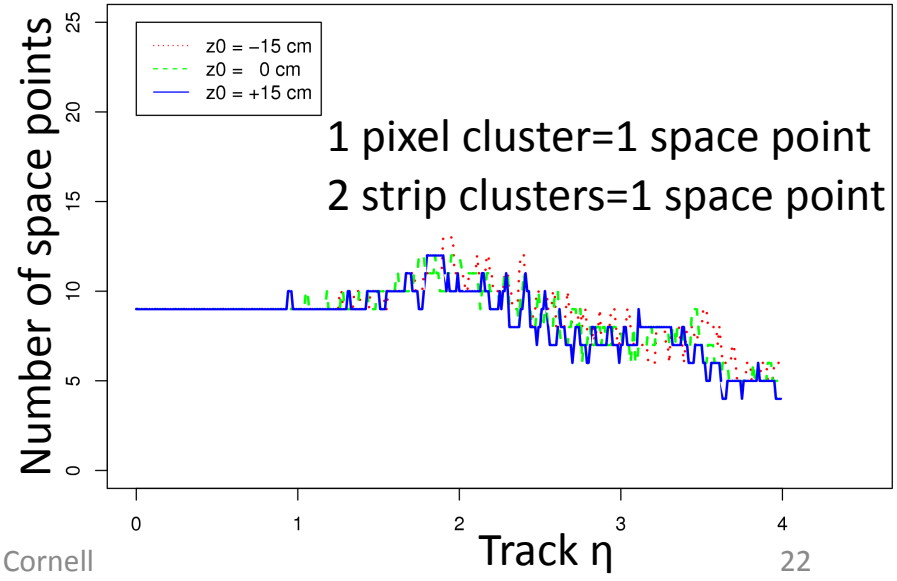
Small Angle Test Beam: Summary

- Long pixel clusters observed: confirmed the concept
- Precise measurement of the incidence angle based on cluster length
  - Essentially the same precision is achieved for 1000e and 2000e thresholds
- Pixel hit efficiency for 50µm pitch along the beam direction is >94%
  - Observed dependence on incidence angle
  - Efficiency strongly degrades with increasing threshold
    - As low as 70% efficiency at 2° incidence angle and 2000e threshold
  - Low thresholds are needed to ensure high pixel hit efficiency
- Charge collection and charge sharing show dependence on reverse bias voltage
- Next steps
  - Compare test beam results with simulation
  - Understand dependence of pixel hit efficiency dependence on incidence angle
  - Test beam studies with irradiated modules

Extended Inner Barrel Layers In Simulation

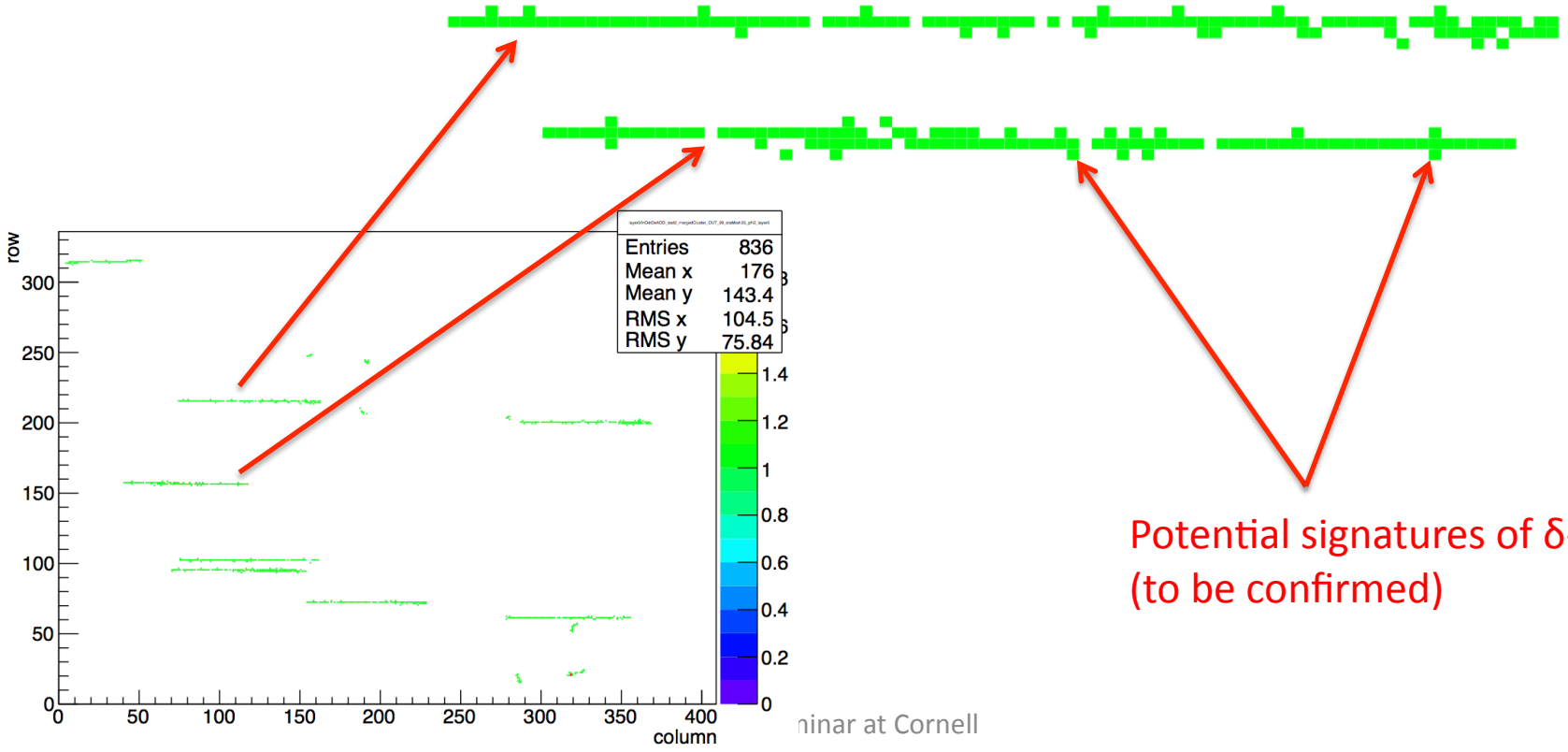
- Simulated layout is used to prove the concept of forward tracking based on the cluster size, to develop software tools and to gain understanding of potential benefits and issues
  - Pixel detector: 4 barrel layers and up to 12 disks on each side
  - (Inner most) Layer-0 coverage up to $|\eta|<4$
  - Pixel pitch: $50 \times 50 \times 150\ \mu m^3$ (Width×Length×Thickness)
  - Electronics threshold at 700e
  - Ttbar sample without pile-up (<μ>=0) and with pile-up (<μ>=50, 100, 200)





Long Pixel Clusters In Simulation

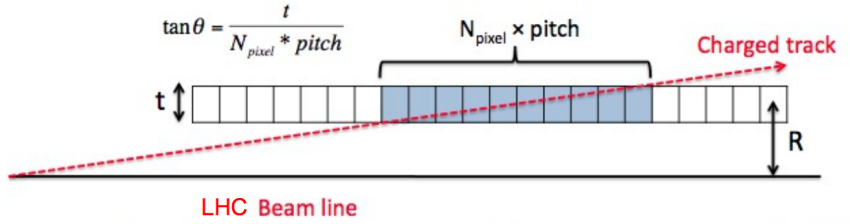
- Example of typical clusters at |η|~4
- Almost every long cluster is broken into several fragments
  - Pixel hit efficiency in simulation to be compared with test beam data
  - Unlike test beam, charge is integrated inside 25ns time window
  - Need clustering algorithm to merge broken clusters
- Efficiency for long clusters is essentially 100%

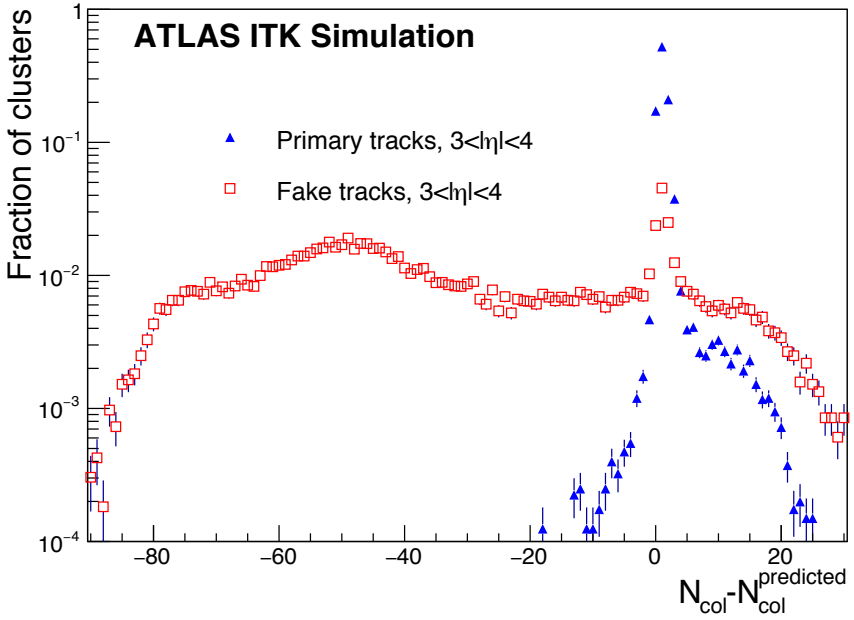


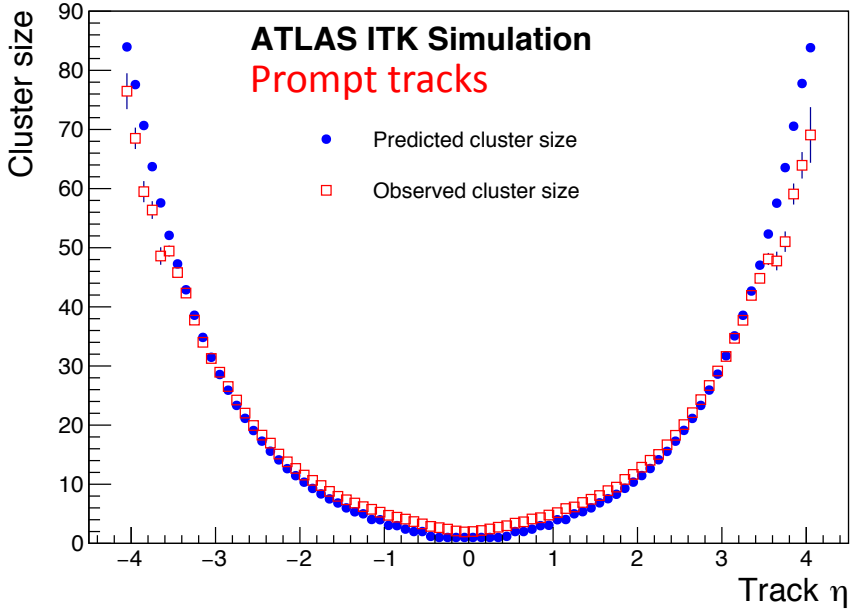
Potential signatures of δ-rays (to be confirmed)

Size Of Pixel Clusters From Prompt And Fake Tracks

- Pixel clusters from prompt tracks follow N_{col}=thickness/(pitch*tanθ) dependence very well
  - Tracks originating from pile-up and secondary interactions follow the same trend
- Most pixel clusters from fake tracks tend to have clusters size incompatible with N_{col}=thickness/(pitch*tanθ) dependence
  - Fake tracks are often made of random combination of pixel clusters

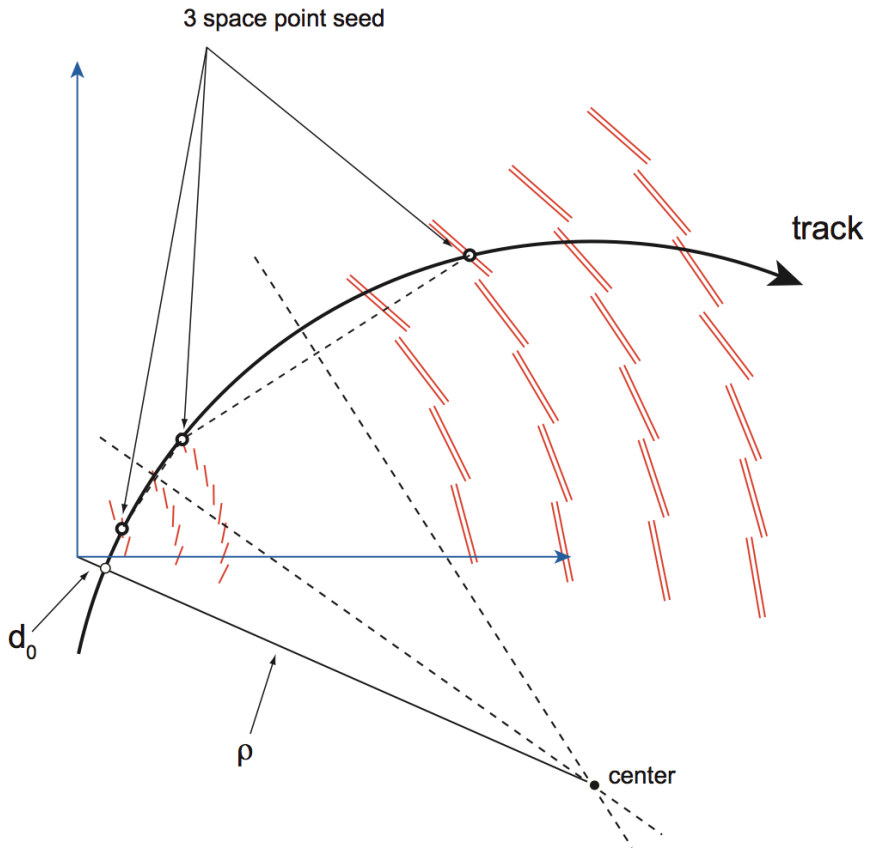






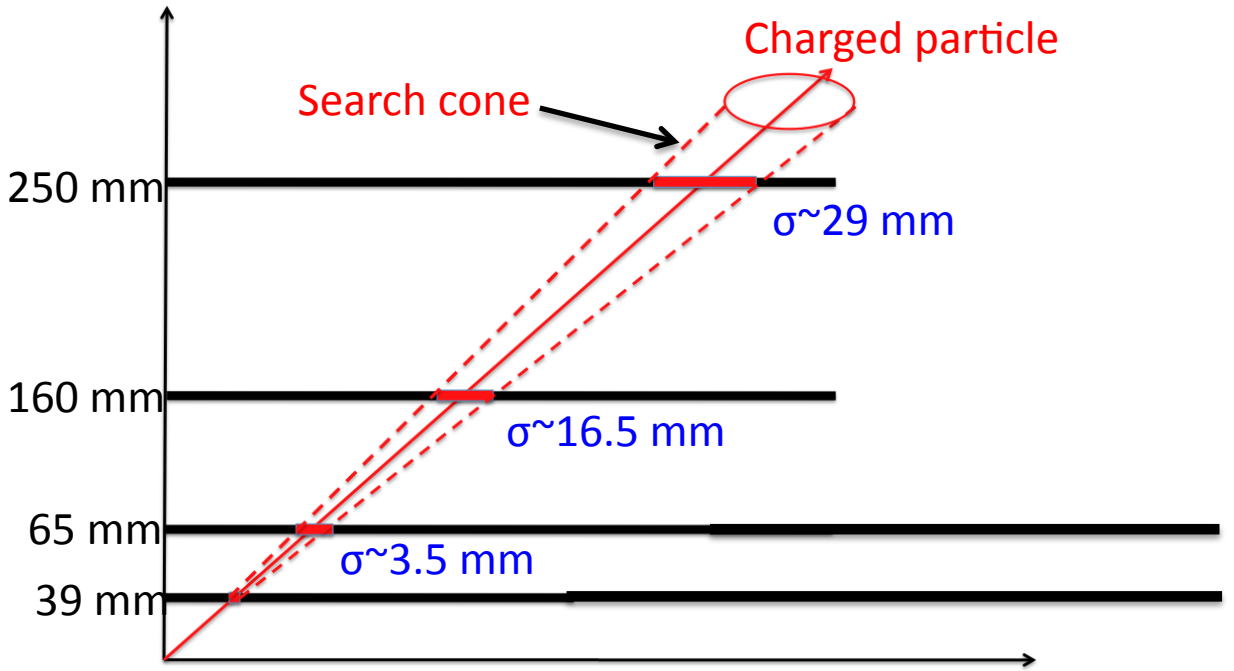
Pattern Recognition At ATLAS

- Track seed= 3 space points
  - Space point provides 3D measurement
    - 1 pixel cluster = 1 space point
    - 2 strip clusters = 1 space point
  - All possible combinations of space points are considered
  - Multiple seeds per track are created
  - Quality cuts applied to reduce number of fake seeds
  - Large number of fake seeds at 200 pile-up interactions
- Seeds provide initial estimates of track parameters
- Search for additional hits along road extrapolated from a seed
- Resolve combinatorial ambiguities due to large number of candidates per track
- Seed creation is most CPU extensive stage of track reconstruction



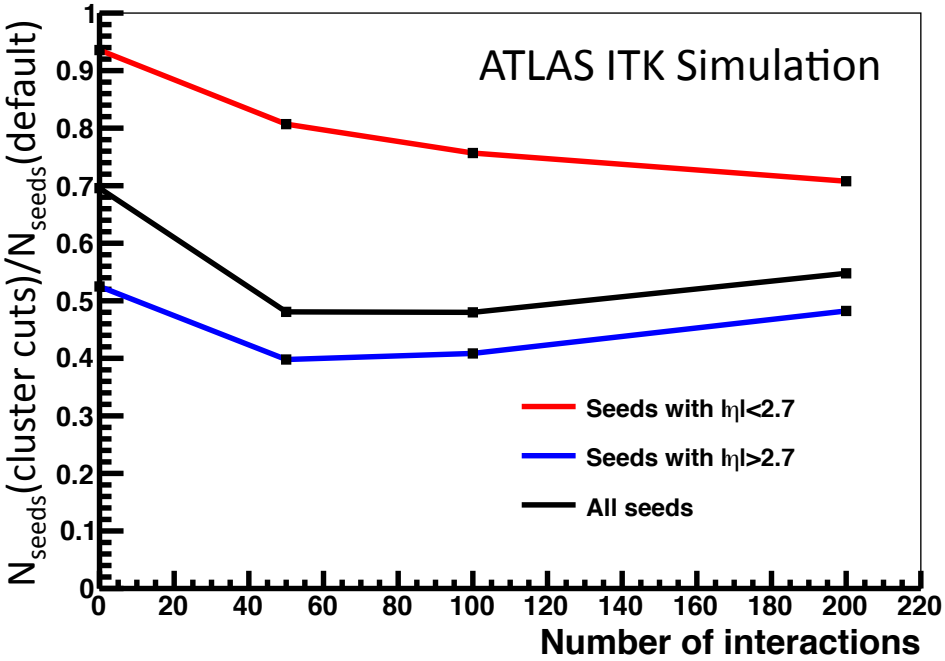
Pattern Recognition Based On Cluster Size: Concept

- **Strategy-1**: reject seeds with pixel clusters whose size is incompatible with θ_{seed}
  - This strategy is currently used in pattern recognition studies
- **Strategy-2**: search for clusters in small cone determined by cluster size in inner layers
  - This strategy potentially offers more advantages (like speed and lower fake rate), but it requires very good understanding and modeling of pixel cluster size
  - To be implemented in the future

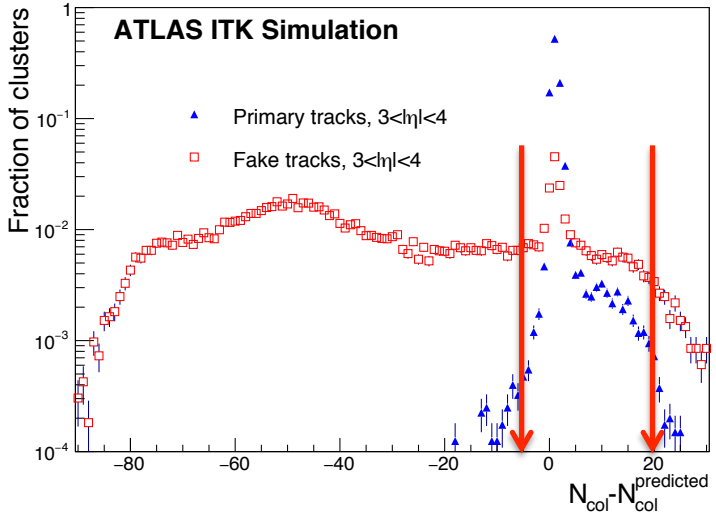


Pattern Recognition Based On Cluster Size: Performance

- About 70% of track seeds in ttbar events with 200 pile-up collisions are in the forward region (|η|>2.7)
  - Seed creation is responsible for ~55% of total CPU time per event
- Cluster size information helps to reduce the number of central (|η|<2.7) and forward (|η|>2.7) seeds by ~30% and ~50%, respectively
  - Reduction in the number of seeds will lead to reduction in CPU time per event

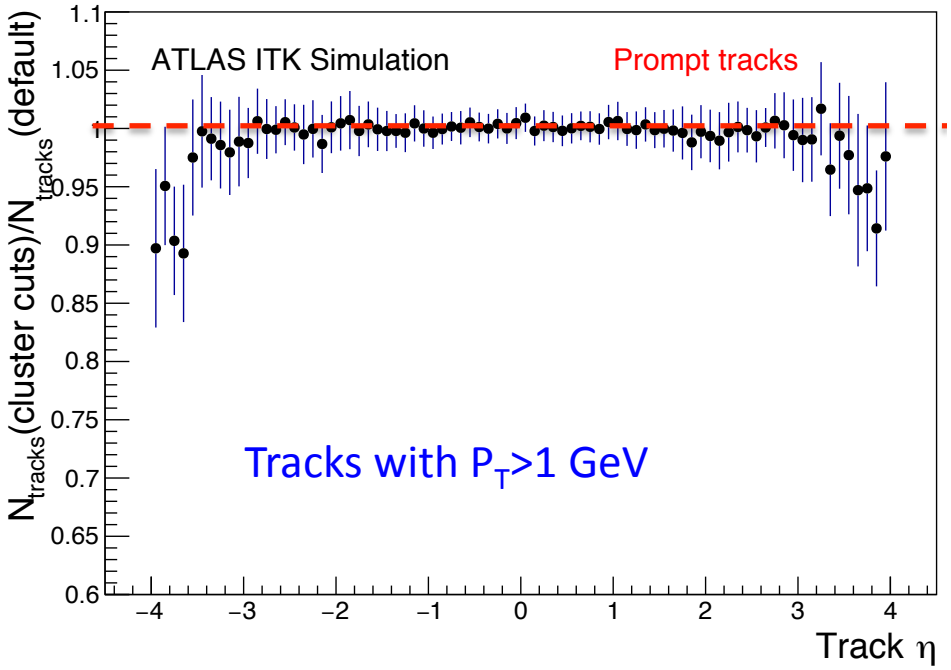


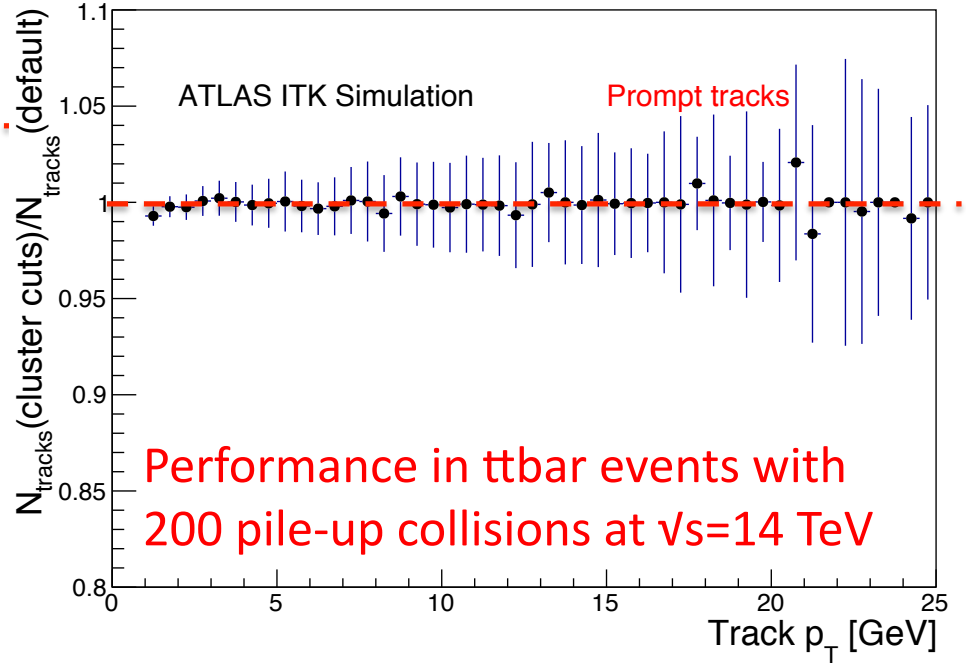
Performance in ttbar events with 200 pile-up collisions at √s=14 TeV



Efficiency For Prompt Tracks

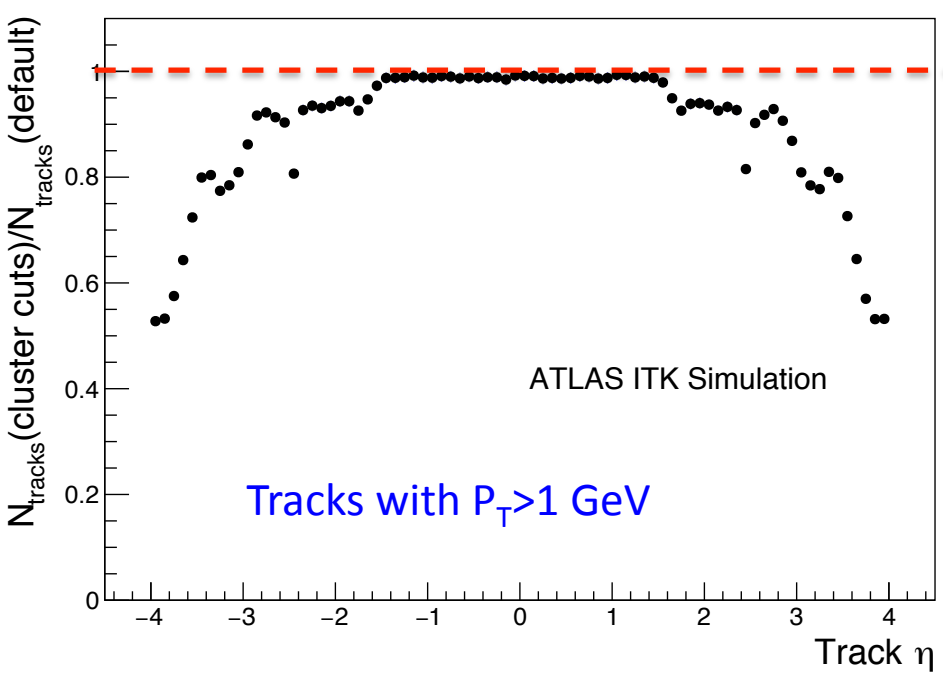
- Large reduction in the number of seeds does not have a significant impact on the number of reconstructed prompt tracks
  - Preliminary results; optimization studies are still in progress
  - N_{tracks}(new): number of tracks reconstructed with pattern recognition exploiting cluster size information
  - N_{tracks}(default): number of tracks reconstructed with default pattern recognition

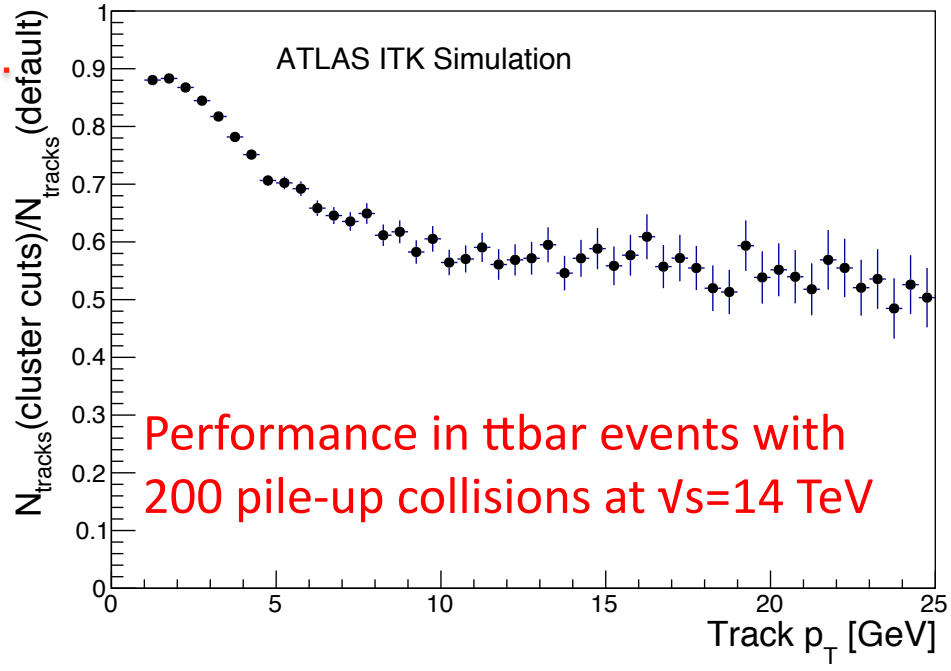




Reduction In The Number Of Fake Tracks

- **Default pattern recognition:** most of the reconstructed tracks in the very forward region (|η|>3.5) are fakes
- **New pattern recognition:** large reduction in the number of fake tracks in the forward region with minimal impact on tracks from hard scattering and pile-up interactions
  - Preliminary results; optimization studies are still in progress





Pattern Recognition With Long Clusters: Summary

- **Long clusters can be used to improve pattern recognition**
- Cluster size in simulation follows predicted pattern
  - Cluster segments can be efficiently merged to restore the original cluster
- Large difference between size of clusters attached to prompt and fake tracks
- Use of cluster size information in pattern recognition allows for significant reduction in the number of seeds and will potentially lead to significant reduction in CPU time
- Reduction in the number of seeds is achieved at a minimal impact on the reconstruction efficiency for prompt tracks
- Use of cluster size information in pattern recognition allows for significant reduction in the number of fake tracks

Conclusions

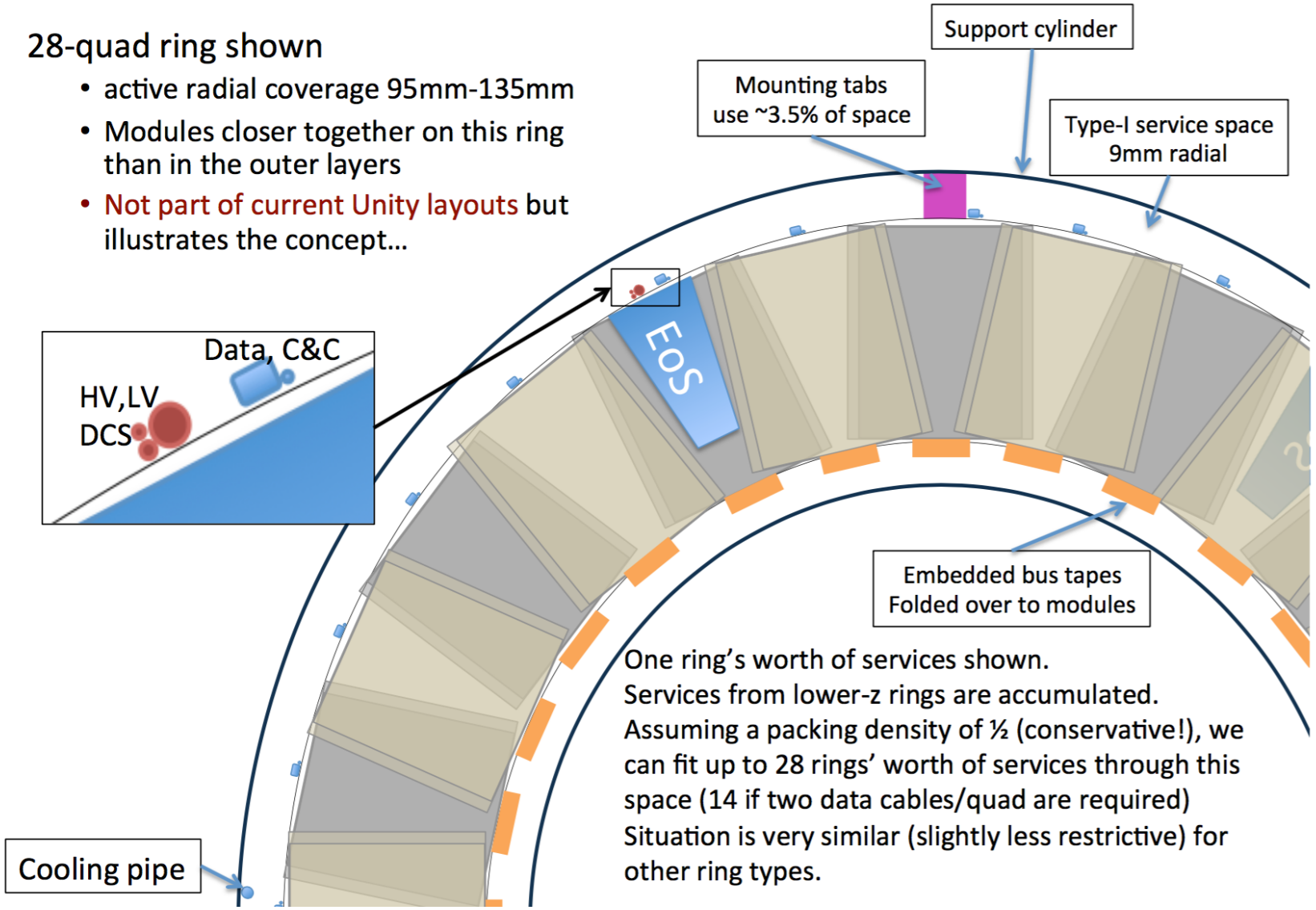
- ATLAS R&D program for Phase-2 all-silicon tracker upgrade is well underway
  - Strip TDR is due in 2016
  - Pixel TDR is due in 2017
- Extensive studies are in progress for the layout of the tracking detector with coverage up to $|\eta|<4$
- Two competing concepts for the Pixel detector layout
  - "Extended" barrel layers
  - "Inclined" barrel modules
- "Extended" barrel layout utilizes cluster size information for improvements in pattern recognition
  - Concept is proven in test beam studies
  - Simulation studies indicate significant benefits for track reconstruction

Backup

End-Cap Pixel Detector

28-quad ring shown

- active radial coverage 95mm-135mm
- Modules closer together on this ring than in the outer layers
- Not part of current Unity layouts but illustrates the concept…



One ring's worth of services shown.
Services from lower-z rings are accumulated.
Assuming a packing density of ½ (conservative!), we can fit up to 28 rings' worth of services through this space (14 if two data cables/quad are required)
Situation is very similar (slightly less restrictive) for other ring types.