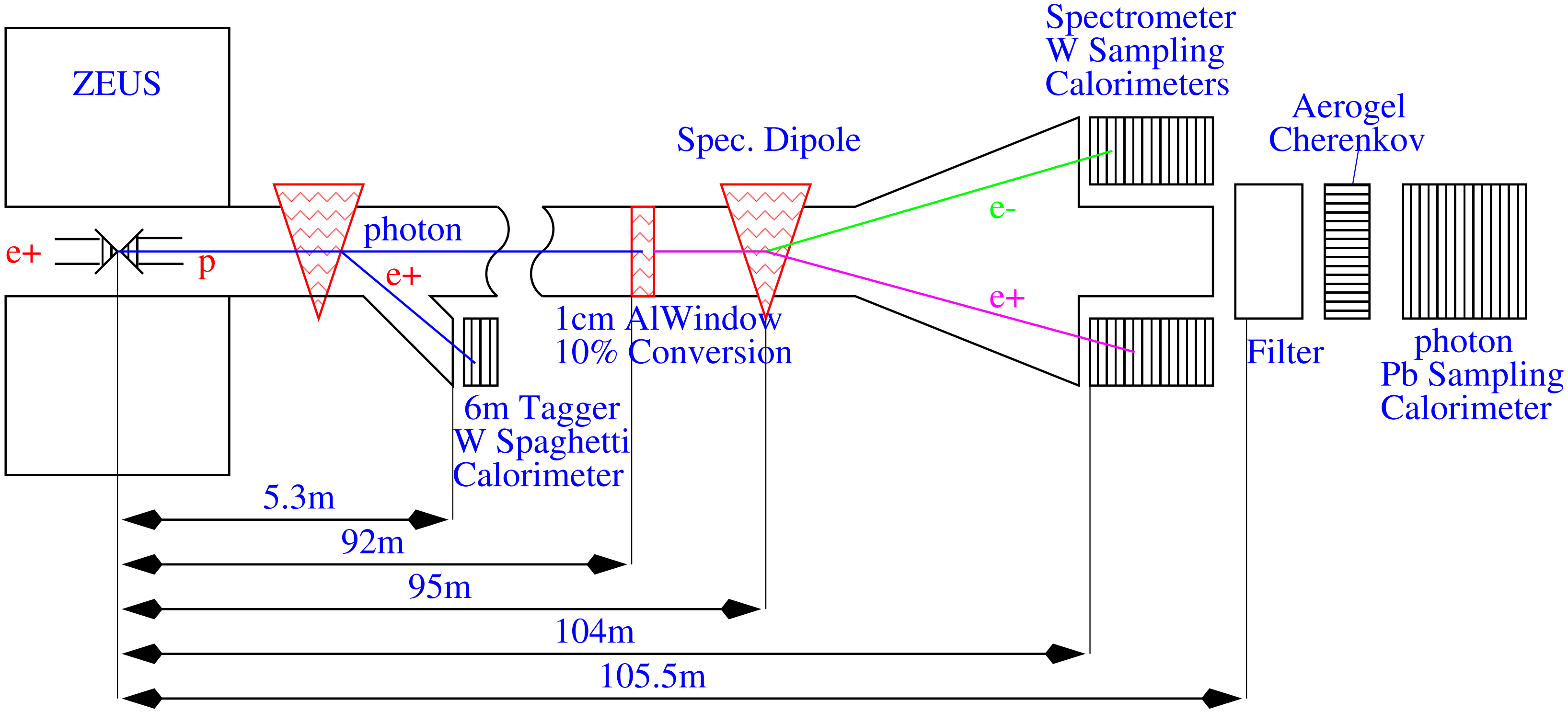
Status of the Electronics



J. A. Crittenden
DESY/ZEUS

The Lumi DAQ

- Front-end analog signal processing and cable driving (100 m)
  Dynamic range and noise definition

- Real-time analysis of data at 10 MHz rate from six detector components spread out over 100 m of beamline:

Component	Z Position	Nr Channels
Electron Calorimeter	-6 m	70
Electron Calorimeter	-40 m	4
e^+e^--pair Calorimeter	-104 m	58
Aerogel Čerenkov	-107 m	2
Photon Calorimeter	-107 m	2
Photon Position	-107 m	30

- Calibration, summing, correlation, fiducial cuts, trigger definitions at this 10 MHz rate

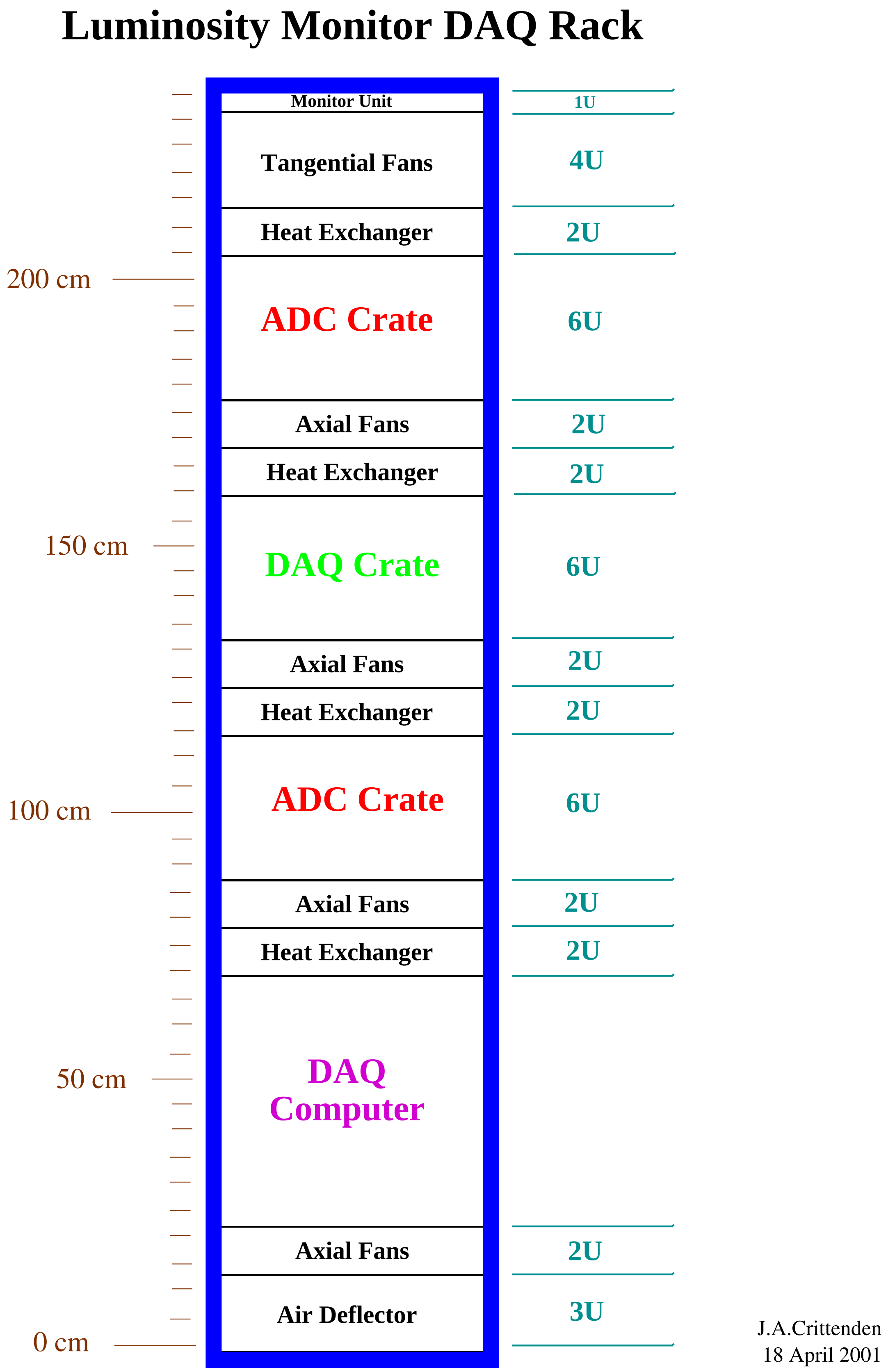
- Provide data to GFLT, SLT, EVB and env. banks

- Provide data to linux PC for on-line calculation and monitoring at $\simeq$ 10 khz rate

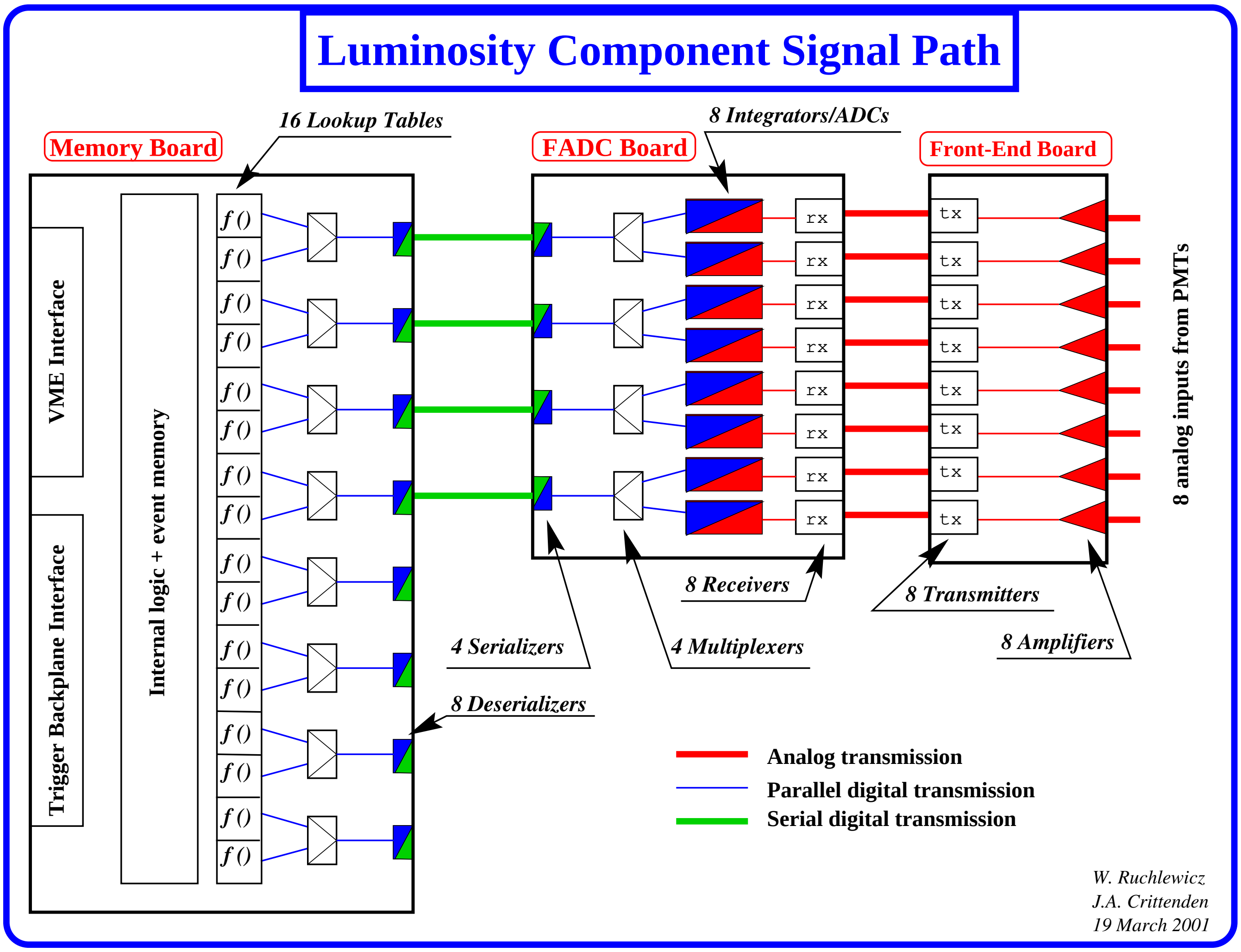
Status of Infrastructure

- All racks, patch panels and cables installed in tunnel and hall
  - $\longrightarrow$ Except for 6m-tagger rack in cryo tower
- DAQ rack now in assembly
  - $\longrightarrow$ Power distribution panel finished and installed
  - $\longrightarrow$ Inergen lines installed
  - $\longrightarrow$ Heat exchangers in place
  - $\longrightarrow$ Water cooling being installed
- All crates available, to be installed as needed

The DAQ Rack in the ZEUS Hall



Signal Path



Luminosity Component Signal Path
Memory Board
16 Lookup Tables
FADC Board
8 Integrators/ADCs
Front-End Board
VME Interface
Trigger Backplane Interface
Internal logic + event memory
f()
rx
tx
8 analog inputs from PMTs
8 Receivers
8 Transmitters
4 Serializers
4 Multiplexers
8 Amplifiers
8 Deserializers
Analog transmission
Parallel digital transmission
Serial digital transmission
W. Ruchlewicz
J.A. Crittenden
19 March 2001

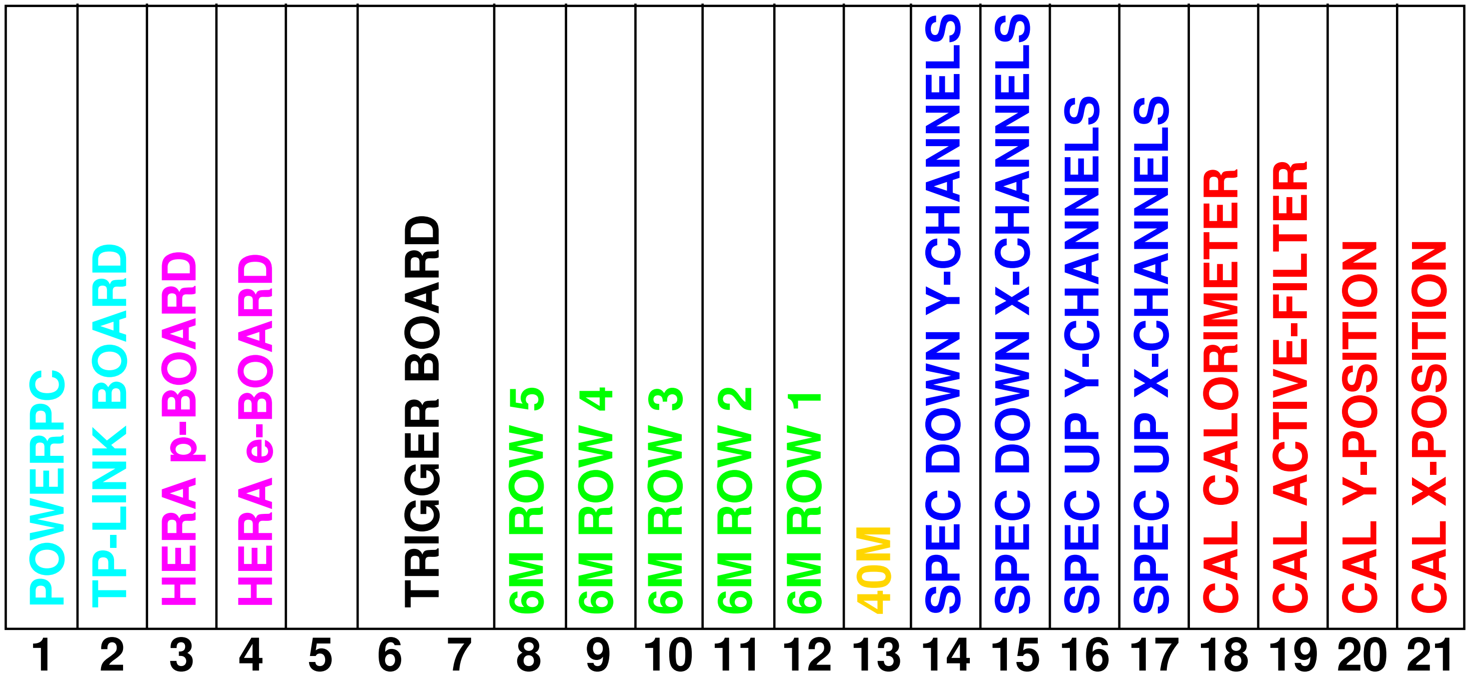
Status of Front End

- 4 Slow-Control units tested, 1 spare in assembly this week
- 1 Fast-Control unit tested, four (1 spare) in assembly this week
- 1 Light- and Charge-Test unit tested, four (1 spare) in assembly
- 1 BBL3 unit tested, four (1 spare) in assembly
- Amplifier boards
  - $\longrightarrow$ Five boards assembled and tested
  - $\longrightarrow$ Remaining PCB's ($\simeq 30$) to arrive this week
  - $\longrightarrow$ Order for assembly by DESY ZE this week
  - $\longrightarrow$ All parts for piggybacks now present
  - $\longrightarrow$ Expect all boards completed by mid-August

Status of Digitizers

- All integrator boards assembled and tested (DESY FEB)
- 3 motherboard PCB's received, 1 assembled and under test
- Expect 5 FADC boards assembled by mid-July
- Order for remaining $\simeq$ 30 boards second week in July
- Expect complete set of boards available by mid-August

The DAQ Crate



INTER-BOARD COMMUNICATION:

- **VME BUS:**
  + POWERPC -> DAQ-BOARDS: RUN PARAMETER
  + TRIGGER -> POWERPC: VME INTERRUPS (DATA READY)
  + DAQ-BOARDS -> POWERPC: EVENT DATA
- **PRIVATE BUS:**
  + TRIGGER -> MEMORY: CLOCK + CONTROL SIGNALS
  + MEMORY -> TRIGGER: ENERGY + POSITION

Status of Memory Boards

- ☞ Extensive testing of prototype (DESY FEA and Cracow)

- ☞ Complete order for PCB's on 13 June

  Delivery expected 2 July

- ☞ Assemble 3 boards by mid-July, ready for use in August

- ☞ Order assembly of remaining boards beginning of August

  Complete set ready by mid-September

Trigger Board Functionality

- **Receive trigger info from MB's**
  - → Pipeline delay for GFLT decision
  - → Compute sums
  - → Define trigger types (See example of 6m-tagger)
  - → Scalers for lumi calculation (pilot bunches, deadtime)
- **Send control signals to MB**
  - → Trigger
  - → GFLT/Local
  - → Bank (switch buffer)
  - → Increment (if no Fast Clear)
- **Provide trigger calculation info to PowerPC**
- **Communicate to/from GFLT**
  - → From: Clock, BNr0, ACCEPT, TType, BCN, GFLTNr, pilot/paired, ...
  - → To: Flags, sums (Physics, KP for 6m-tagger, ...)
- **Generate charge- and light-test triggers**
- **Generate clock to FADC controller**

The red stuff is not on the present trigger board.

It was originally planned to build a second module for these purposes.

Results of Tests on the Present Trigger Board

- Trouble with serial transmission of MB trigger info
  - ⟶ Desynchronization errors
    Rate depends on crate position and nr MB's present
  - ⟶ Reducing termination resistor from 100Ω to 27Ω changed symptoms but no solution
- Logical functionality extensively tested: works!
  - ⟶ FPGA test modes
  - ⟶ VME interface
  - ⟶ Read/write all registers
  - ⟶ Read/write memories (word mode, block mode)
  - ⟶ Both main and auxiliary FPGA's
  - ⟶ Code debugging (pipeline, data formatting, adders)

Continuing tests and development

- Improve serial transmission
- Subtrigger definition
- Scalers
- Trigger definition for MB (prescaling)

Motivation for Single-Board Design

☞ Fix layout of serial transmission receivers

- → Independent ground plane
- → Trace routing (crosstalk)
- → Distance of receivers from connector

☞ Avoid duplication of receivers

☞ Increase depth from 160mm to 220mm to match crate

☞ Ensure modularity with piggybacks

Spares of all parts can be made within a few weeks following commissioning

☞ Obviate need for second trigger board

Avoid double-loading serial transmission

Time Schedule

Trigger board ordered on 12 June

Delivery expected end of July

Two weeks for programming, testing

⇒ Ready for operation mid-August

In the meantime, ...

- ☞ Test improvements to serial transmission (twisted pairs, backplane modifications, etc)
- ☞ FPGA programming development

Very serious manpower problem

- ☞ Prepare ancillary board for minimum functionality

Insurance against the Unforeseen
Two-day leadtime

⟶ Need HERA clock, BNr0, pilot/paired info from GFLT

⟶ Send clock to FADC controller

⟶ Present TB gets trigger sum from single MB (photon cal), reads out three MB (photon cal, position detector)
Requires 3 MB, 5 FADC boards, 5 Frontend boards

Summary

Assembly and commissioning of all DAQ components now underway

DAQ system sufficient for beam-position monitoring and on-line luminosity estimation planned for mid-August

Complete DAQ system expected by mid-September