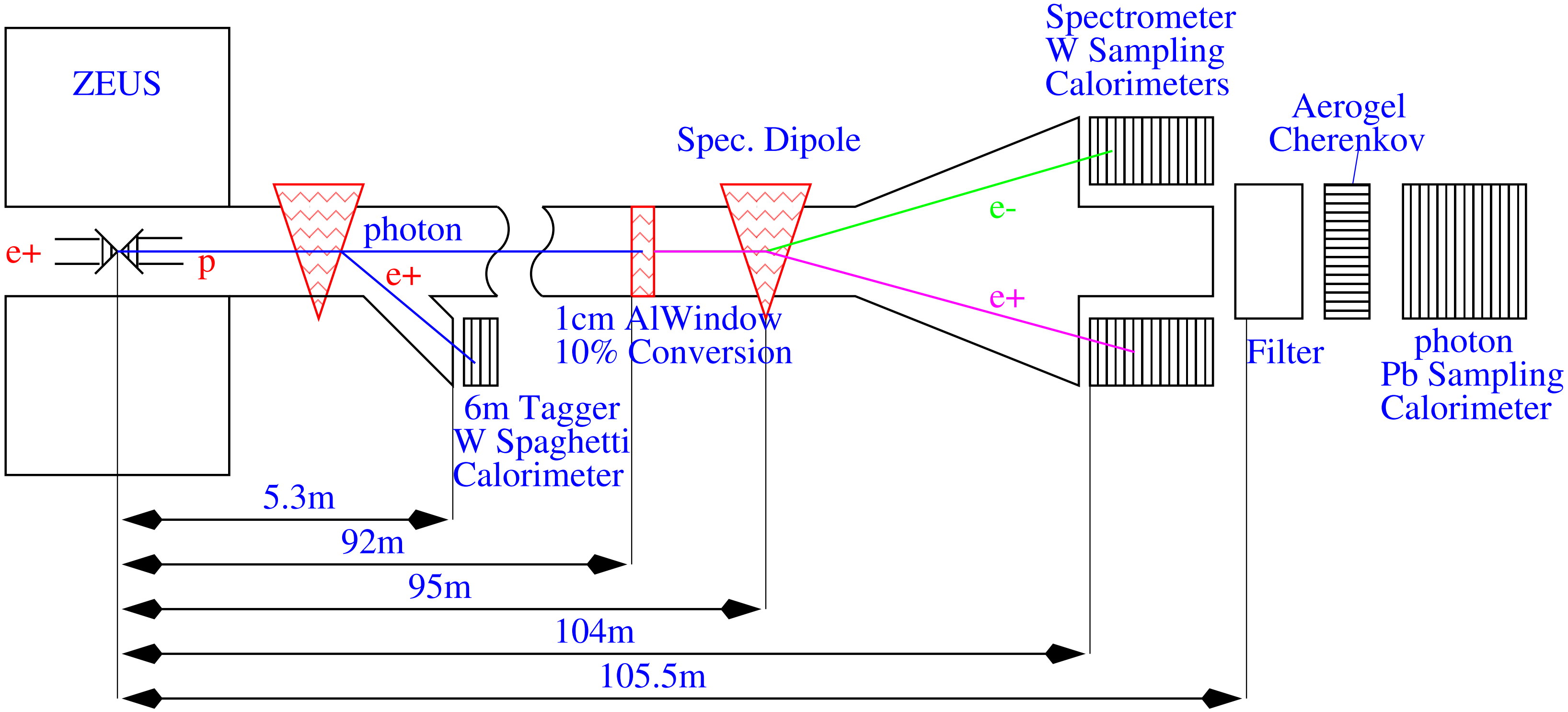
Status of the Electronics



The Challenge

☞ Front-end analog signal processing and cable driving (100 m), dynamic range and noise definition

☞ Real-time analysis of data at 10 MHz rate from six detector components spread out over 100 m of beamline:

Component	Z Position	Nr Channels
Electron Calorimeter	-6 m	70
Electron Calorimeter	-40 m	4
e^+e^--pair Calorimeter	-104 m	58
Aerogel Čerenkov	-107 m	2
Photon Calorimeter	-107 m	2
Photon Position	-107 m	30

☞ Calibration, summing, correlation, fiducial cuts, trigger definitions at this 10 MHz rate

☞ Provide data to GFLT, SLT, EVB and env. banks

☞ Provide data to linux PC for on-line calculation and monitoring at $\simeq$ 10 khz rate

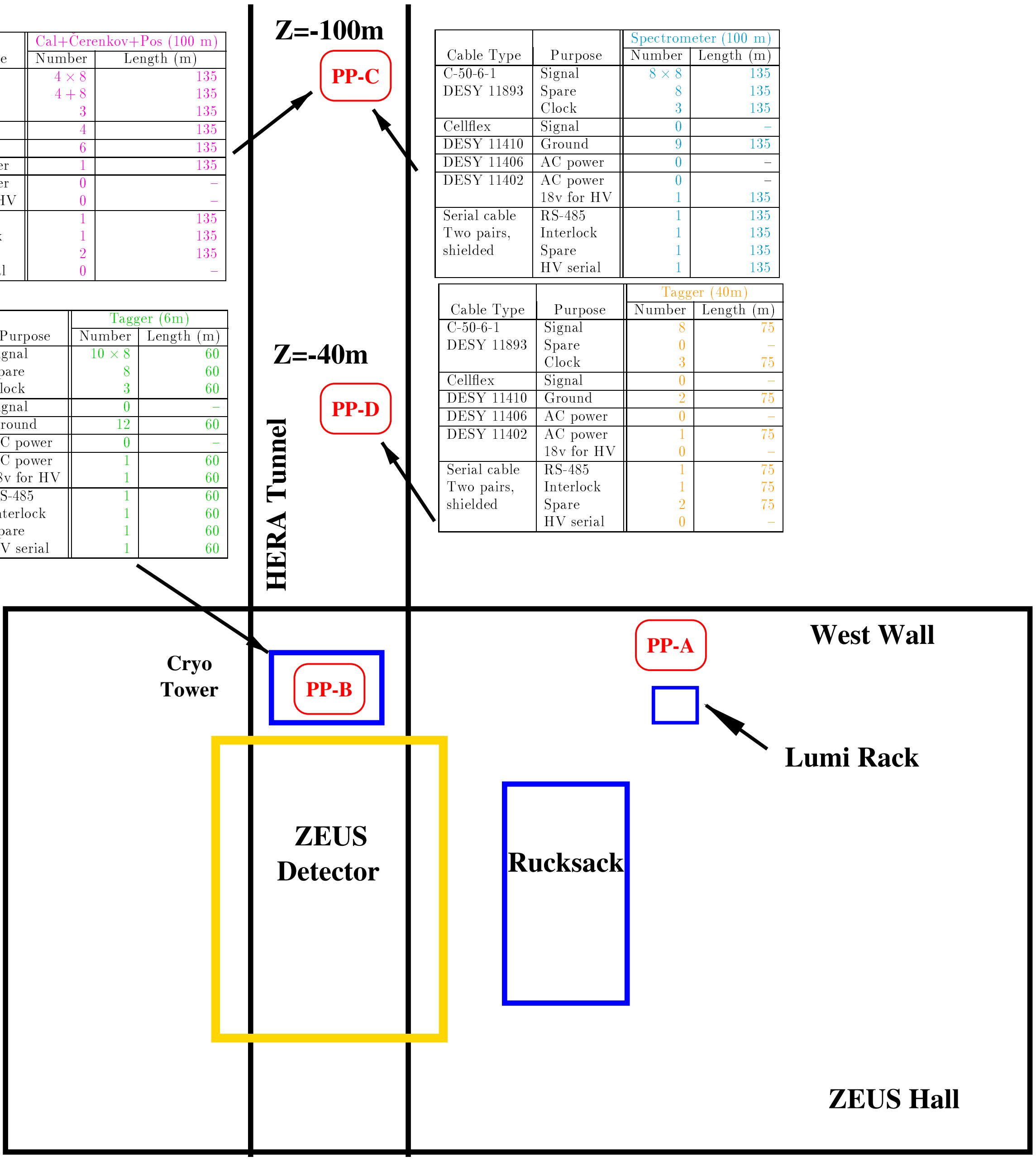
The Infrastructure (I)

Cable Type	Purpose	Cal+Cerenkov+Pos (100 m) Number	Length (m)
C-50-6-1 DESY 11893	Signal	4×8	135
	Spare	$4+8$	135
	Clock	3	135
Cellflex	Signal	4	135
DESY 11410	Ground	6	135
DESY 11406	AC power	1	135
DESY 11402	AC power	0	–
	18v for HV	0	–
Serial cable Two pairs, shielded	RS-485	1	135
	Interlock	1	135
	Spare	2	135
	HV serial	0	–

Cable Type	Purpose	Spectrometer (100 m) Number	Length (m)
C-50-6-1 DESY 11893	Signal	8×8	135
	Spare	8	135
	Clock	3	135
Cellflex	Signal	0	–
DESY 11410	Ground	9	135
DESY 11406	AC power	0	–
DESY 11402	AC power	0	–
	18v for HV	1	135
Serial cable Two pairs, shielded	RS-485	1	135
	Interlock	1	135
	Spare	1	135
	HV serial	1	135

Cable Type	Purpose	Tagger (6m) Number	Length (m)
C-50-6-1 DESY 11893	Signal	10×8	60
	Spare	8	60
	Clock	3	60
Cellflex	Signal	0	–
DESY 11410	Ground	12	60
DESY 11406	AC power	0	–
DESY 11402	AC power	1	60
	18v for HV	1	60
Serial cable Two pairs, shielded	RS-485	1	60
	Interlock	1	60
	Spare	1	60
	HV serial	1	60

Cable Type	Purpose	Tagger (40m) Number	Length (m)
C-50-6-1 DESY 11893	Signal	8	75
	Spare	0	–
	Clock	3	75
Cellflex	Signal	0	–
DESY 11410	Ground	2	75
DESY 11406	AC power	0	–
DESY 11402	AC power	1	75
	18v for HV	0	–
Serial cable Two pairs, shielded	RS-485	1	75
	Interlock	1	75
	Spare	2	75
	HV serial	0	–



The Infrastructure (II)

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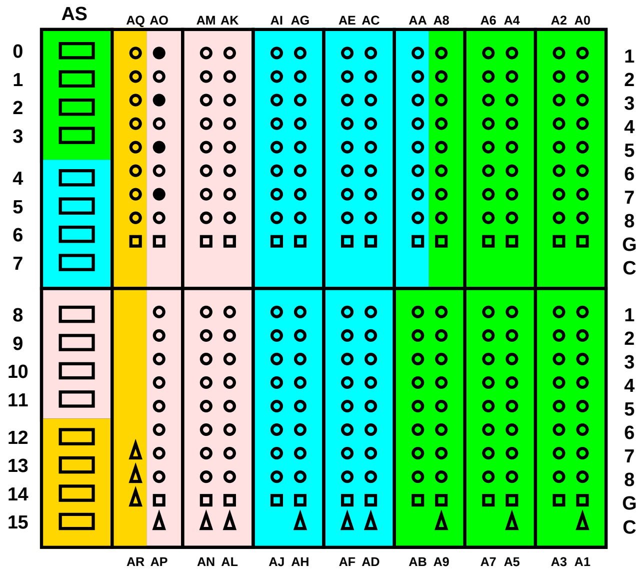
February 25, 2001

Luminosity Component Cables
– Between HERA Tunnel and ZEUS Hall –

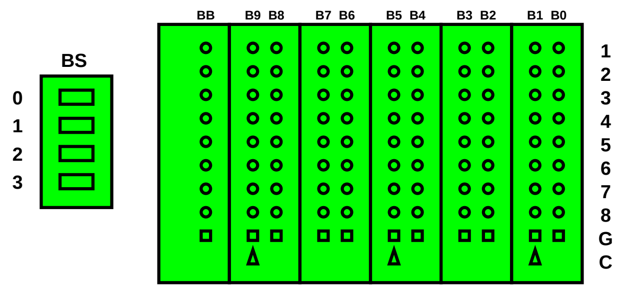
Cable Type	Purpose	Cal+Čerenkov+Pos (100 m)		Spectrometer (100 m)		Tagger (40m)		Tagger (6m)	
		Number	Length (m)	Number	Length (m)	Number	Length (m)	Number	Length (m)
C-50-6-1	Signal	4×8	135	8×8	135	8	75	10×8	60
DESY 11893	Spare	$4 + 8$	135	8	135	0	–	8	60
	Clock	3	135	3	135	3	75	3	60
Cellflex	Signal	4	135	0	–	0	–	0	–
DESY 11410	Ground	7	135	9	135	2	75	12	60
DESY 11406	AC power	1	135	0	–	0	–	0	–
DESY 11402	AC power	0	–	0	–	1	75	1	60
	18v for HV	0	–	1	135	0	–	1	60
Serial cable	RS-485	1	135	1	135	1	75	1	60
Four pairs,	Interlock	1	135	1	135	1	75	1	60
shielded	Spare	2	135	1	135	2	75	1	60
	HV serial	0	–	1	135	0	–	1	60

The Infrastructure (III)

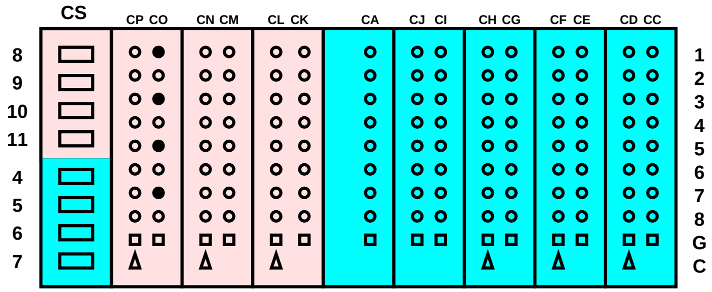
Patch Panel A (ZEUS Hall)



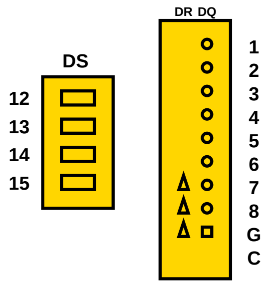
Patch Panel B (6m Tagger)



Patch Panel C (Tunnel 100 m)



Patch Panel D (Tunnel 40 m)



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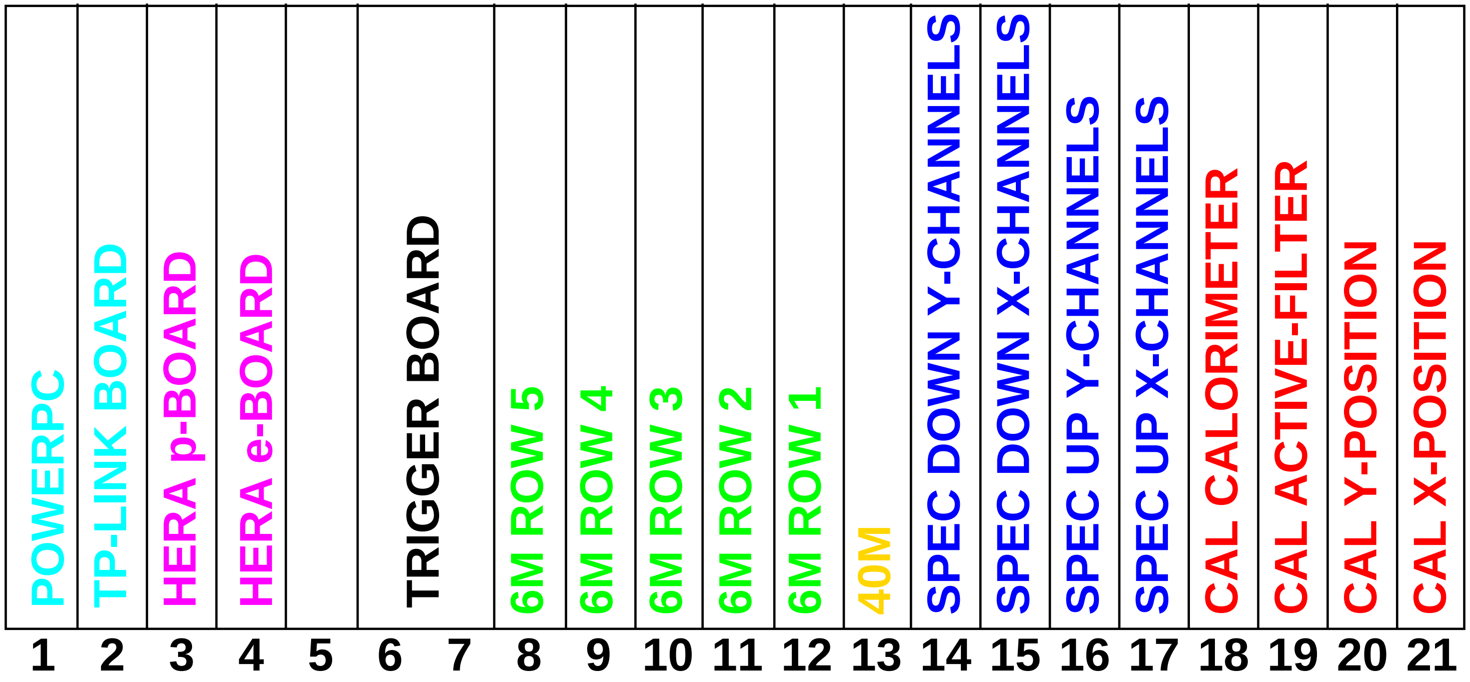
The DAQ Crate



INTER-BOARD COMMUNICATION:

- **VME BUS:**
  + POWERPC -> DAQ-BOARDS: RUN PARAMETER
  + TRIGGER -> POWERPC: VME INTERRUPS (DATA READY)
  + DAQ-BOARDS -> POWERPC: EVENT DATA

- **PRIVATE BUS:**
  + TRIGGER -> MEMORY: CLOCK + CONTROL SIGNALS
  + MEMORY -> TRIGGER: ENERGY + POSITION

The Plan

☞ Infrastructure

Cabling and patch panels ready in 2-3 weeks;

DAQ rack and power distribution panel ready by end March

☞ Front End

Crates, Slow control units, Fast control units plus one amplifier/driver module per crate installed by May;

Thorough bench testing continues, installation during short accesses

☞ FADC boards

2nd integrator prototype tested, PCB's ordered;

Motherboard PCB's ordered, fabrication in March and April

☞ Memory boards

2nd prototype under test, PCB's to be ordered end February, fabrication in April

☞ Trigger board

Under construction in Warsaw, delivery in March

The Conclusions

☞ Nervous Times ("Put up or shut up")

☞ Tunnel infrastructure in progress, ready by end March

☞ Front-end limited by delivery times:

Will need short accesses to install tested amplifier/driver modules

☞ Can expect DAQ operational by end of May

(Much software development remains $\Rightarrow$ Talk by WR)

☞ Foreseeable bottleneck:

Programming of FPGA's for calibration and trigger

Heroic efforts underway