The Trigger Board for the Upgraded Luminosity Monitor DAQ

- ☞ **Overview of the Lumi DAQ**
- ☞ **Functionality of Trigger Board**
- ☞ **Trigger Board Tests**
- ☞ **New Design**
- ☞ **Time Schedule**

J. A. Crittenden *DESY/ZEUS*

The Lumi DAQ

- Front-end analog signal processing and cable driving (100 m), dynamic range and noise definition

- Real-time analysis of data at 10 MHz rate from six detector components spread out over 100 m of beamline:

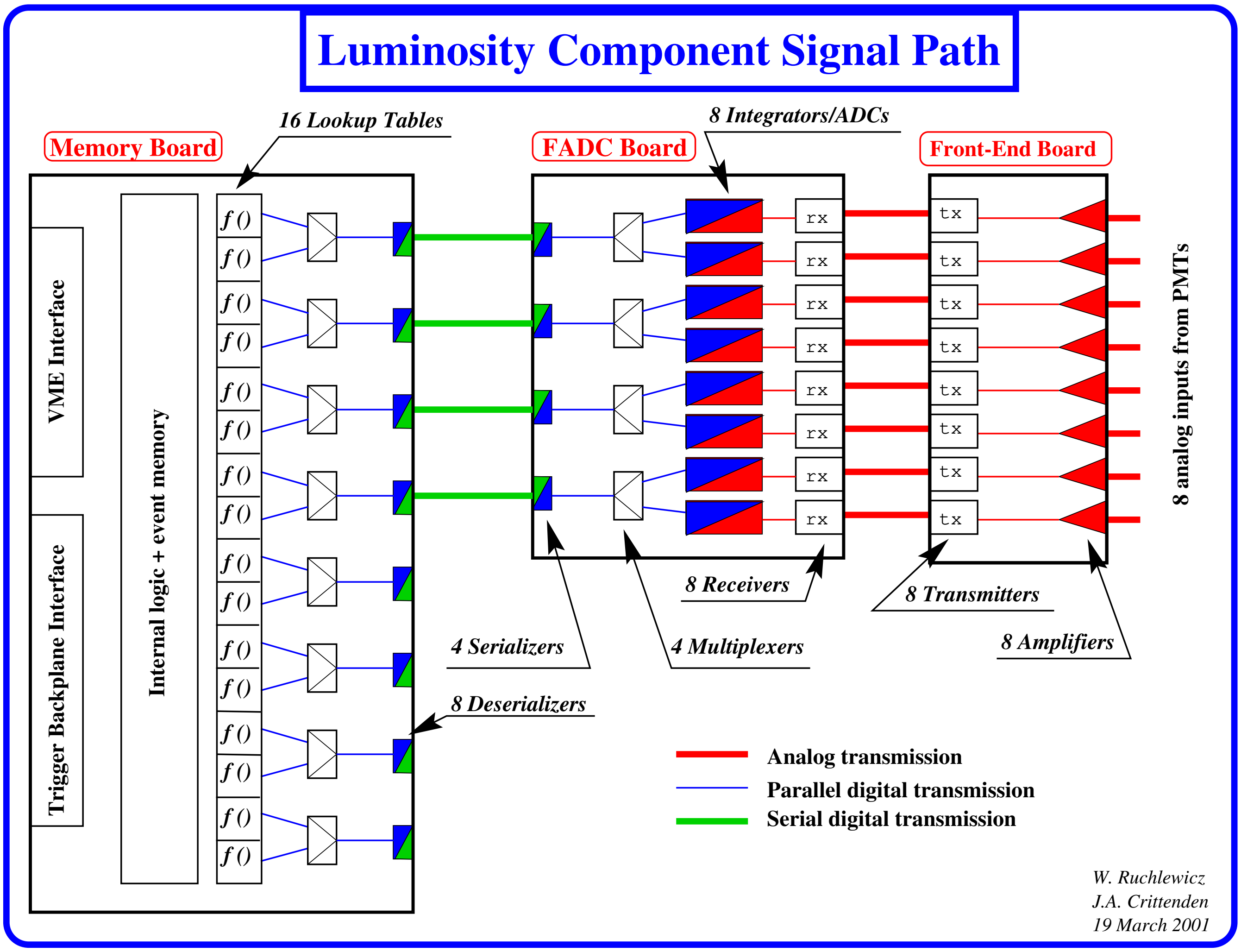
Component	Z Position	Nr Channels
Electron Calorimeter	-6 m	70
Electron Calorimeter	-40 m	4
e^+e^--pair Calorimeter	-104 m	58
Aerogel Čerenkov	-107 m	2
Photon Calorimeter	-107 m	2
Photon Position	-107 m	30

- Calibration, summing, correlation, fiducial cuts, trigger definitions at this 10 MHz rate

- Provide data to GFLT, SLT, EVB and env. banks

- Provide data to linux PC for on-line calculation and monitoring at $\simeq$ 10 khz rate

Signal Path



Luminosity Component Signal Path
Memory Board
16 Lookup Tables
FADC Board
8 Integrators/ADCs
Front-End Board
VME Interface
Trigger Backplane Interface
Internal logic + event memory
f()
rx
tx
8 analog inputs from PMTs
8 Receivers
8 Transmitters
4 Serializers
4 Multiplexers
8 Amplifiers
8 Deserializers
Analog transmission
Parallel digital transmission
Serial digital transmission
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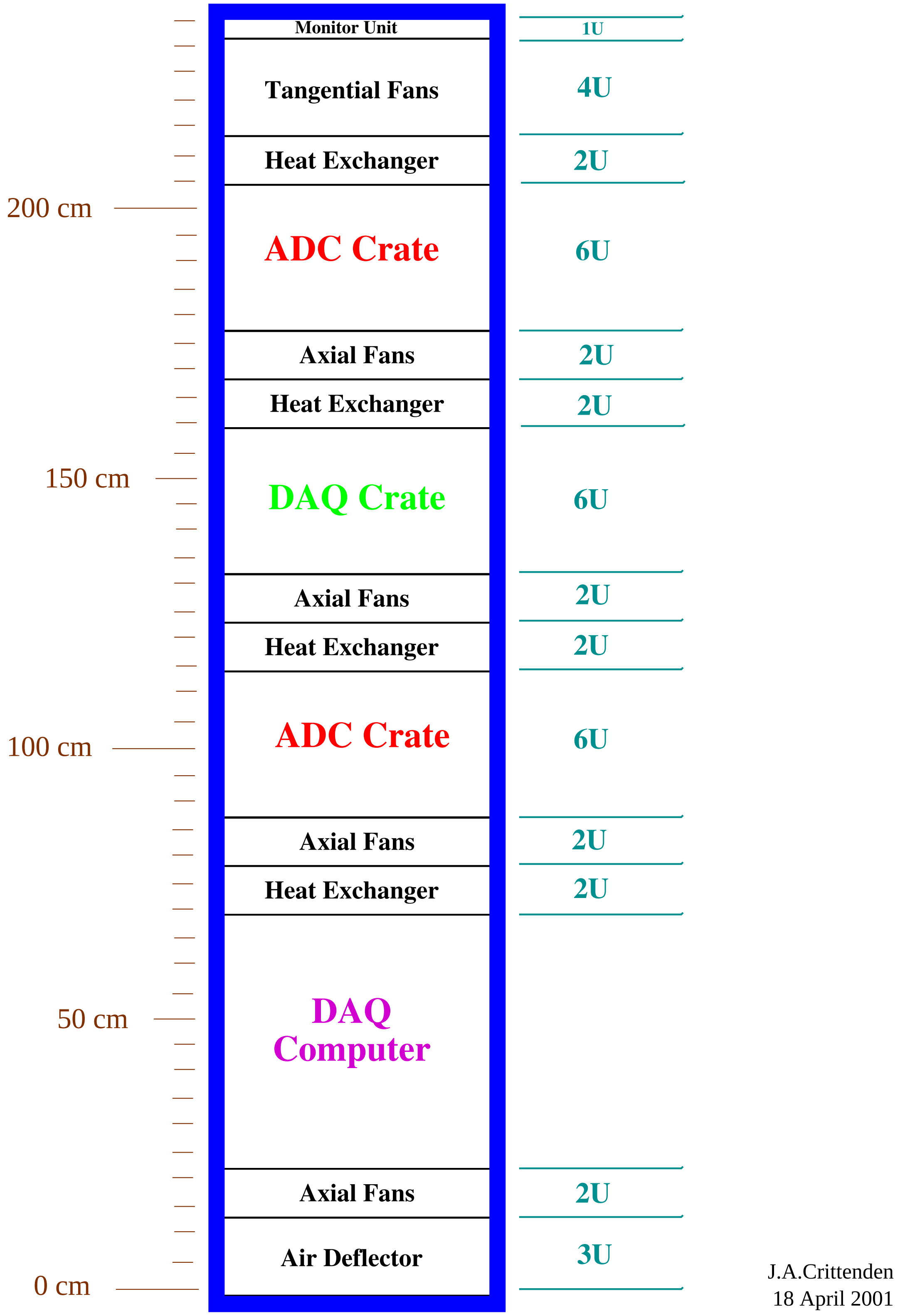
19 March 2001

The DAQ Rack in the ZEUS Hall

Luminosity Monitor DAQ Rack



The DAQ Crate

Slot	Board
1	POWERPC
2	TP-LINK BOARD
3	HERA p-BOARD
4	HERA e-BOARD
5	
6 7	TRIGGER BOARD
8	6M ROW 5
9	6M ROW 4
10	6M ROW 3
11	6M ROW 2
12	6M ROW 1
13	40M
14	SPEC DOWN Y-CHANNELS
15	SPEC DOWN X-CHANNELS
16	SPEC UP Y-CHANNELS
17	SPEC UP X-CHANNELS
18	CAL CALORIMETER
19	CAL ACTIVE-FILTER
20	CAL Y-POSITION
21	CAL X-POSITION

INTER-BOARD COMMUNICATION:

- **VME BUS:**
  - + POWERPC -> DAQ-BOARDS: RUN PARAMETER
  - + TRIGGER -> POWERPC: VME INTERRUPS (DATA READY)
  - + DAQ-BOARDS -> POWERPC: EVENT DATA
- **PRIVATE BUS:**
  - + TRIGGER -> MEMORY: CLOCK + CONTROL SIGNALS
  - + MEMORY -> TRIGGER: ENERGY + POSITION

Trigger Board Functionality

- **Receive trigger info from MB's**
  - ⟶ Pipeline delay for GFLT decision
  - ⟶ Compute sums
  - ⟶ Define trigger types (See example of 6m-tagger)
  - ⟶ Scalers for lumi calculation (pilot bunches, deadtime)
- **Send control signals to MB**
  - ⟶ Trigger
  - ⟶ GFLT/Local
  - ⟶ Bank (switch buffer)
  - ⟶ Increment (if no Fast Clear)
- **Provide trigger calculation info to PowerPC**
- **Communicate to/from GFLT**
  - ⟶ From: Clock, BNr0, ACCEPT, TType, BCN, GFLTNr, pilot/paired, ...
  - ⟶ To: Flags, sums (Physics, KP for 6m-tagger, ...)
- **Generate charge- and light-test triggers**
- **Generate clock to FADC controller**

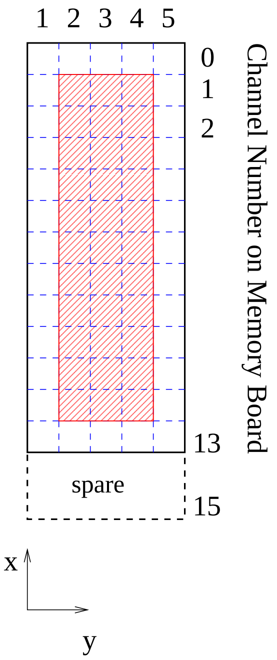
The red stuff is not on the present trigger board.

It was originally planned to build a second module for these purposes.

Trigger Algorithm for 6m Tagger

6m-Tagger Trigger Proposal

Memory Boards:



TagEnTot = SUM(i=1,5) TagEn_i

Trigger Types:

1-5) TagTr_j = TagEnLow_j < TagEnTot < TagEnHigh_j   j=1...5

5 Windows on Total Energy of Tagger for Bremsstrahlung & KP

=> 5*2 Constants (10*7bit?)

Fiducial Volume:

a) TrEn_n > TrEn_i   i= 1...5   n = y-coordinate (3 bit)

TagMax_n = 0...15 = x-coordinate (4 bit)

b) Look-up Table: 5x16 bit -> image of tagger in memory

loadable as 'constant' from outside to ADRoffset

ADRoffset+xxxyyyy
0000000

ADRoffset+xxxyyyy
1011111

```
00000000000000ss
01111111111110ss
01111111111110ss
01111111111110ss
00000000000000ss
```

1: fiducial volume
0: outside cells
s: spare

6) TagTr_6 = bit(ADRoffset+xxxyyyy)   => 80bits

7) 5-bit constant SW to switch on fiducial volume trigger (6) for any of the energy triggers (1-5)   => 5 bit

Total 6mTagger Trigger:

TagTr = OR(j=1,5) [TagTr_j and (not bit(j, SW) or TagTr_6)]

total number of 'constant' bits: 155

Results of Tests on the Present Trigger Board

- ☞ Trouble with serial transmission of MB trigger info
  - ⟶ Desynchronization errors
    Rate depends on crate position and nr MB's present
  - ⟶ Reducing termination resistor from 100Ω to 27Ω changed symptoms but no solution
- ☞ Logical functionality extensively tested: works!
  - ⟶ FPGA test modes
  - ⟶ VME interface
  - ⟶ Read/write all registers
  - ⟶ Read/write memories (word mode, block mode)
  - ⟶ Both main and auxiliary FPGA's
  - ⟶ Code debugging (pipeline, data formatting, adders)

Continuing tests and development

- ☞ Improve serial transmission
- ☞ Subtrigger definition
- ☞ Scalers
- ☞ Trigger definition for MB (prescaling)

Motivation for Single-Board Design

- Fix layout of serial transmission receivers
  - → Independent ground plane
  - → Trace routing (crosstalk)
  - → Distance of receivers from connector
- Avoid duplication of receivers
- Increase depth from 160mm to 220mm to match crate
- Ensure modularity with piggybacks

  Spares of all parts can be made within a few weeks following commissioning
- Obviate need for second trigger board

  Avoid double-loading serial transmission

Time Schedule

Order trigger board TOMORROW

Receive it in 7 weeks (end of July)

Two weeks for programming, testing

$\Rightarrow$ Ready for operation mid-August

In the meantime, ...

- ☞ Test improvements to serial transmission (twisted pairs, backplane modifications, etc)
- ☞ FPGA programming development

Very serious manpower problem

- ☞ Prepare ancillary board for minimum functionality

Insurance against the Unforeseen
Two-day leadtime

$\longrightarrow$ Need HERA clock, BNr0, pilot/paired info from GFLT

$\longrightarrow$ Send clock to FADC controller

$\longrightarrow$ Present TB gets trigger sum from single MB (photon cal), reads out three MB (photon cal, position detector)

Requires 3 MB, 5 FADC boards, 5 Frontend boards