7-8-68

Addenda #1

DVM Interface to Computer and Energy-Meter Display

A card-file of electronics auxiliary to the main frame of the DVM proper has been installed immediately above the local readouts (labeled panel #1 in the text). This card-file contains two subsystems of the DVM, one being interfacing circuitry between the DVM and the computer, the other being circuitry to drive incandescent lamps for the energy-meter display permanently assigned to DVM channel #3. See interface block diagram #DH3973.

DVM interfacing to the computer is necessary to provide a means of recording various voltage values as read by the DVM and subsequently using these computer-recorded values in computer programs, allowing analysis of various synchrotron parameters. All parameters measured by the DVM may not be useful in machine analysis, although provisions are made to send the information from any DVM channel (channels #3 through #44 only) to the computer. The input to the computer from the DVM is a 14 bit word containing any voltage level of the 4000 step staircase generated in the DVM. The computer is instructed to read, on command, one selected DVM channel at a time and when a readout cycle is occurring in the DVM for a particular channel, the corresponding BCD staircase values are set into a register, the output of which is transferred into the computer under program control.

Referring to the block diagram for the interface unit, card #1 converts a binary input from the computer to a modified decimal code used for channel selection. Cards #2, 3, and 4 AND this modified decimal code with the DVM's CFF pulses to produce a pulse occurring at the time the computer-selected channel is being read out by the DVM. This special pulse sets a flip-flop whose output strobes a column of flip-flops on card #5, setting these flip-flops to the corresponding staircase voltage which appears at the input of the computer. Before another channel can be read by the computer, a reset pulse must be sent to the interface from the computer to reset the strobe-producing flip-flop.

Card #6 is a current amplifier to provide higher output currents and isolation from the DVM's BCD scaler outputs.

Another function of the interface unit is to generate high currents to drive an incandescent lamp display for the synchrotron energy readout. The cards involved are #7, 8, 9, and 10. The block diagram shows these cards being fed from the DVM BCD current-amplifier, card #6. Cards #7, 8, and 9 convert the DVM's BCD outputs to decimal outputs for the units, tens, and hundreds lamps in the lamp display module. Card #10 provides only a one-thousand output as the lamp display is only required to display a maximum number of 1000 representing 10.00 GEV from the synchrotron. The decimal point in the display is always stationary and is provided by the display itself.

A pulse from the DVM's channel #3 CFF output is used for strobing the storage flip-flops in cards #7 through 10, meaning that only channel #3's (synchrotron energy) output will be delivered to the lamp display module.

Supply voltages for this card cage come from two sources. One source is standard synchrotron-electronics supply-voltages (+15, +6, -6, -15) which must be connected up to the standard-electronics power-supply connector at the rear of the card cage. The other power-supply required is +5 volts for the integrated circuits, supplied from a separate power-supply located at the rear, bottom of the DVM cabinet; (see schematic #AH3970).

The lamp display uses #44 bayonette lamps. Ten lamps are illuminated at synchrotron energies less than 10 GEV and eleven lamps at 10 GEV. The total lamp current is about 2 amps at roughly 5.5 volts and a separate adjustable power supply is used for the display; (see schematic #AH3974).

As a result of installing the GEV readout display and the computer interface electronics, the panels are not as numbered on page 2 of the DVM description.

The order of the panels now is:

Top panel	-	GEV display
2nd "	-	Blank
3rd "	-	Local nixie readouts
4th "	-	Computer interface logic
5th "	-	Odd inputs 23 through 44
6th "	-	Comparators 23 to 44
7th "	-	Even inputs 24 through 44, Odd inputs 1 through 21, Input selector switches
8th "	-	Comparators 1 to 22
9th "	-	Even inputs 2 through 22
10th "	-	Logic
11th "	-	Output switches and remote Bipco connectors
12th "	-	Main power supply
13th "	-	Input signal-cable patch panel

Addenda #2

Measurement and Display of A.C. Line Voltage

A special Bipco module is used for the display of A.C. line voltage. (See schematic CH3972.) This particular readout module must not be interchanged with a standard readout module as shown on CH3968.

A.C. line voltage is measured by transforming the 115 VAC line 1:1, half wave rectifying and filtering the transformer's output and providing precision adjustment of the resulting D.C. voltage. This D.C. output voltage is purposefully selected to be 1.000 volts above the output voltage from a temperature-compensated reference diode. In this case, the reference diode output = +6.214 and the adjustable incoming D.C. set to +7.214 volts. These two D.C. voltages are used as the differential input of an operational amplifier with a gain of -4.000.

The resulting output of the op-amp (negative 4.000 times the differential input) is fed to a 3-digit D.V.M. channel whose output feeds the special Bipco unit mentioned above.

An input voltage of -4.000 volts to the D.V.M. would ordinarily produce a Bipco reading of 1600. The special module has the K's Bipco replaced with a Nixie bulb connected to display "1" only, the K's input connected to the 100's Bipco, 100's input connected to the 10's Bipco, 10's input connected to the 1's Bipco.

The A.C. line-voltage card's calibration (see #BH3423) is adjusted such that 116.0 VAC line voltage reads 1160 on the special module, calibrated by adjusting the 100 ohm pot on the line voltage card.

Measured accuracy is ± .1 volt from 105 VAC to 125 VAC.

Addenda #3

The DVM was originally designed for use with a very low source-impedance input signal. The input impedance of the comparators is 24.0 K, requiring the source impedance to be less than 6 ohms in order to approach the 0.025% accuracy of the instrument. With a finite source-impedance above a few ohms, an error in instrument linearity occurs, the amount of error being a function of the source-impedance and input bias current. A special circuit has been added to each comparator input to compensate for input bias current and, therefore, correct scale non-linearities. See schematic #AH3971.

The input-offset-current (input bias) is zeroed-out by the following method:

1. Short input of comparator of desired channel.
2. Adjust voltage offset pot on that comparator board so that channel output reads 0000.
3. Set up integrator-calibrator box and external resistance decades for 216.000 K ohms in series with integrator-calibrator's internal supplies.
4. Connect commercial DVM to calibrator's output-terminal voltage terminals.
5. Set calibrator voltage to 95.00 volts (DVM should read 3800) and later to 5.00 volts (DVM should read 0200) while calibrating each channel.

6. Adjust 50 K pot in offset circuit for scale of numbers.
7. Adjust 1 K pot in offset circuit for range of numbers.
8. Repeat above steps until commercial DVM and 44 channel DVM agree in voltage.

After input-offset-current compensation (calibration) is completed, the source impedance can be in the megohm range while instrument linearity is maintained within accuracy limits.