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# MAGNET POWER FOR THE CORNELL ELECTRON SYNCHROTRON

## Introduction

The Cornell Electron Synchrotron has an effective radius of curvature of 98.7 meters. It is a fast cycling machine which presently operates at 60 Hz. The magnets are capable of operation to about 20 GeV. The magnets are connected in a White[1] series resonant circuit except that there is no central power distributing transformer. There are 192 magnet and 4 quadrupole modules each with a transformer and resonating capacitors; these components are mounted on the individual magnet support beams. The module transformers are fed through a ring busbar system also housed in the support beam structure. (See Figure 1 for a condensed magnet connection diagram.)

For the AC component of the magnet power, sinusoidal rather than pulse excitation is preferred to reduce the distribution losses in the extended feed system. Also, reduction of the harmonic content in the drive waveform will minimize the excitation of delay line modes of the magnet circuit. Delay line modes (due to various causes) have proven to be a definite, but manageable, problem. The AC magnet power supply operates with about 15% harmonic content in the drive current when the machine is in the sinusoidal mode. Flat-topping is envisaged and will, of course, dramatically increase the harmonic content.

We have taken advantage of technological advances to construct an inverter-type AC supply using only solid-state components, rather than ignitrons. Such a supply is efficient, flexible, quiet, economical, and takes a minimum of space.

For the projected excitation to 15 GeV the AC power requirement is one megawatt of single phase power at 600 VAC and 60 Hz. This is derived from the three phase line in the following steps:

1. Three phase 13.4 kV power transformed to two three phase stars (180° out of phase with one another) with a line to line voltage of 270 Volts.

2. SCR controlled rectification in two rectifiers whose outputs are in series.

3. LC filtering of the outputs of the two rectifiers. Note in Figure 2 that only the center tap of the filter capacitors is grounded.

4. Inversion by solid state DPDT switches[2] (inverters).

5. Filtering of the square wave (voltage) output of the inverters by series resonant circuits. The switches are commutated by the reactive power in the series filters which are tuned somewhat above 60 Hz for this purpose.

Figure 3 is a schematic of one of the inverters (which act as a DPDT switch as shown in Figure 2).

DC magnet power is supplied by six supplies spaced around the ring with only one supply regulated. They are electrically in series with the magnets of the ring.

## Inverter Operation

When a diagonal pair of SCRs is triggered, current rises and falls as befits a series resonant load. When the current reverses, the diodes in parallel with the SCRs conduct. The other SCR pair may then be triggered and a reverse cycle of current through the load begins.

The load conditions under which the current will reverse within the required time (1/120 sec.) are of interest. The steady state condition is simple, the load must be capacitive at 60 Hz. That is to say, the load must be tuned to a frequency greater than 60 Hz.

Even under steady state conditions, the load cannot be adequately represented as a simple series resonant circuit. Figure 4 shows an equivalent circuit sufficient for steady state analysis. Because the current $I_{in}$ from the inverter is reasonably free from harmonic content, it is convenient to consider only the fundament component, $V_{in}$, of the square-wave voltage applied to the equivalent load.

Figure 4 shows the parallel resonant magnet load as equivalent to a conductance G in parallel with an admittance $\Psi$. The admittance represents the amount of mistuning of the magnet load. (It is normally about 45° inductive.) The phasor diagram relates $V_{in}$ to the magnet load voltage $V_o$. In practice, $\Psi$ varies with temperature and line frequency while $L_1$, $C_1$, and G do not vary significantly.

To first order, we desire a certain value for $V_o$ and then ask under what conditions ($V_{in}$, $L_1$, $C_1$, etc.) we can obtain this value for $V_o$.

The load $V_{in}/I_{in}$ seen by the inverter will be capacitive if:

$$\Upsilon \equiv \left(\frac{1}{\omega C_1} - \omega L_1\right)\left(G\right) \text{ is greater than } \tfrac{1}{2}$$

It will commutate only if:

$$Q^* \equiv \left(G^2 \frac{L_1}{C_1}\right)^{\frac{1}{2}} \gtrsim 1$$

If Q* is large, the stored energy in $L_1C_1$ is expensive. For our operation, $1.2 < Q^* < 1.6$ is attractive.

Figure 5 is a plot of $V_{in}/V_0$ (times some constant) vs. the phase angle of the magnet load for various values of $\gamma$. Normal operation (for $\gamma \doteq 1$) is made by starting with the magnet load nearly in tune (phase angle about 20° inductive). As the resonating capacitors warm up, the tuning becomes more inductive and operation stabilizes somewhere near the minimum in the curve (phase angle about 45° inductive).

It is important to operate near the minimum in the curve where $V_0$ is 90° out of phase with respect to Vscr. This is the region in which the magnet current is independent of the line frequency. (Note that the inverter triggers are generated and timed by signals derived from the power line and that they can be applied to the SCRs only if various conditions, including reverse current in the diodes, are satisfied.) Variations in the line frequency, though small, are difficult to compensate for rapidly. These variations appear as effective changes in the phase angle of the magnet load. Near the minimum, the resultant variations in the magnet voltage (and thus current) are minimized. Power line voltage variations can readily be quickly compensated for in a voltage regulation loop in the rectifiers which preceed the inverters.

We have tried to use a circuit (phase-locked oscillator with high apparent Q) to smooth out the variations in line frequency. However, such a system was not effective because, over a few tens of cycles (the minimum time for effective correction), it was possible for the magnet phase to drift beyond the allowable limits for proper timing of the RF used for acceleration. (The RF being tied to the line phase.)

Analysis of behavior of the currents in the system upon turn-on is difficult, therefore, our "analog computer" was a prototype inverter powering 8 magnets to 10 GeV. We found that the system was stable for $\gamma \gtrsim 0.7$ and for Q*'s between 1.2 and 2.0. At the start of operation the conduction angle of the SCRs oscillates about the steady-state value with a period of a few tenths of a second. The oscillations damp to the steady state value in about one second. Operation, where possible, below $\Upsilon = 0.5$ shows a much less damped, and occasionally anti-damped, behavior.

If the magnet load is suddenly shorted (crowbarred), the inverter current changes largely in phase and not in magnitude. We could use this happy accident to drain energy from the magnet ring upon detection of a fault.

Figure 6 is a plot of the electrical phase angle $\Phi$ through which the diodes (in parallel with the SCRs) conduct. It is plotted vs. the "mistuning" of the magnet ring for various values of the parameter $\Upsilon$. Note that in the region of normal operation, the conduction phase angle is more or less independent of the "magnet mistuning". This fact has some connection with the ease with which the system may be turned on. One may consider either that upon turn-on the frequency is indefinite or that the magnet load's phase varies as the magnets fill with energy over the first half second of operation.

The magnet ring modules are actually tuned quite carefully to present an impedance to the feed system which is in tune at 10 GeV and slightly capacitive below. The inductive "mistuning" is intentional and is effected by inductors across the feed lines at the output of the supply.

Figure 7 shows the output current of the inverter vs. time for typical operating conditions. The discontinuities each 180° are rounded over a period of about 100μ seconds.

## Softening Networks

Figure 8 shows the details of the SCR modules shown in Figure 3. The purposes of the modules are:

1. To limit the initial rate of current rise upon turn-on of the SCR.

2. To keep high frequency spikes from appearing between the terminals of the SCR. Such spikes can cause the device to trigger; the gate-anode capacity provides a mechanism.

3. To limit the rate of rise of the voltage upon turn-off of the diode. When the diagonal pair of SCRs fires, the diode current drops off at a rate limited by: $(V_{dc}/L)$, where L is the sum of the inductors in series with the supply voltage. The turn-off process takes about 100 microseconds. At the end of this period, the SCR voltage rises at a rate limited largely by the softening network. The diode's stored charge is also significant.

Ferrite cores are used to form the inductors. The bus bar to the anode of the SCR passes through the ferrite cores forming an inexpensive and quiet saturable reactance with a frequency response useful to about 500 kHz where the core losses become conveniently large.

Delay Line Modes

The many magnet modules, all in series, have stray capacitances to ground forming a delay line. The period of the delay line around the machine is about 5 milliseconds. Standing voltage waves may be excited by harmonic components in the magnet supply current. The capacitive currents to ground caused by the delay line modes upset the equality of current around the ring. This effect is particularly critical at injection time when the magnet excitation current is instantaneously low; very small quadrature unbalance currents excited by the full drive amplitude then assume importance. The probable excitation of delay line modes and the desire to keep feed-line losses small are important reasons for having chosen a near-sinusoidal excitation system.

We have made provision for damping the delay line modes. This has been done by insulating the cases of the resonating capacitors and then connecting them to ground through a resistor. In this way, part of the stray capacitance has a low effective Q. Initial tests did not indicate difficulties with the delay line modes. However, it did become obvious that they caused difficulties early in the acceleration cycle when operating at high peak excitation. The beam bump and the DC supplies generate traveling waves of larger magnitude than those produced by the AC excitation.

## Control Logic

The control logic for the inverter and start cycle is described in the 3750 series of drawings. Some salient features of the system are:

1. Veto signals. These signals are generated by fault detection circuits. Upon detection of a fault, all SCR triggers are stopped. For example, if the interlock chain is broken for any reason, all further SCR triggers are stopped so that the rectifiers will not be drawing current when the main contactor opens (many tens of milliseconds later).

2. Inverter protection. In order for inverter SCR triggers to be generated, it is necessary that a signal be generated by reverse current flowing in the diodes which parallel the SCRs in the inverter. In this circuit, the generated signal charges a capacitor which provides the supply voltage for a transistor in the final stages of amplification of the SCR trigger rather than as a gate at some earlier point. Of course, to start the system, the signal must be simulated.

3. Additional inverter protection. Also required for continued inverter operation are signals indicating that the SCRs have fired. The presence of this signal insures that, should an SCR fire out of turn such that two SCRs are effectively placed across the DC supply, then such a failure will be detected. Upon detection of such a failure, a crowbar (section entitled Crowbar for Inverter) is activated which can clear the SCRs before damage has occurred.

4. Slow start system. This system assures the correct turn-on sequence. In particular, the rectifiers are not started until after the contactor is closed and the transients in the line voltage have ceased. The inverter is started as the rectifier output voltage slowly rises. The regulation loop is designed so that the turn on is gentle while stabilization is achieved within 30 seconds.

5. Rectifier protection. Serious damage to the filter capacitors is possible if the rectifiers should come on suddenly. The voltage on the filter capacitors could become twice the maximum output voltage of the rectifiers. In order to protect the capacitors, a circuit detects the rate of rise of the rectifier voltage and can shut off the rectifiers before the stored energy in the filter choke is sufficient to damage the filter capacitors. In addition, direct overvoltage protection is provided as well as protection against the rectifier output voltage dropping too rapidly. It has been observed that if the output of the rectifiers decreases too rapidly, it is possible for the inverter SCRs to fire when the conditions are not correct. This occurs most often when the DC magnet power supply drops out and the system is operating in the (normal) slope regulation mode.

## Crowbar for Inverter

The inverters are effectively four single-pole single-throw switches sequenced to act as a double-pole, double-throw reversing switch. (See Figure 9.) The load impedance is of the order of one ohm. A limiting choke of about 40 microhenries is in series with the supply. Its purpose is to limit the rate of current rise in the switches (SCRs). Its impedance is of the order of 20 milliohms at 60 Hz. Its impedance must be kept reasonably low so that the stored energy in it will be small compared to the energy absorbed by the load per cycle. Suppose that $S_1$ should fire accidentally while $S_2$ and $S_3$ were conducting at $t = t_o$. The current in $S_1$ will rise at a rate of E/L Amps/sec. We could turn off $S_1$ by closing $S_5$. $S_5$ would rob $S_1$ of current as well as reverse the voltage across $S_1$ sufficiently to clear the SCR. Clearly, the problem is to then turn off $S_5$. The solution is to place a capacitor in series with $S_5$ and to pre-charge the capacitor so that $S_5$ will starve the inverter of current and will also reverse the direction of current through the faulted leg of the inverter for a sufficient length of time to allow any healthy SCR to clear. (It is not clear if this method will protect $S_2$ if $S_1$ should short out completely. During the time of the crowbar, the load current will remain essentially constant. The peak currents in $S_5$ are about 2500 Amperes which is sufficient to clear $S_2$ at full load in most cases.)

The inductor, $L_f$ is used to limit the rate of rise of the current in $S_5$. It is essential that $S_5$ be triggered in a very vigorous manner to prevent its deterioration. $S_5$ must also be protected so that if it should fire under normal operating conditions, dI/dt will be limited to a safe (or at least reasonable) value.

At the present time, there is a circuit whereby all eight of the inverter SCRs in the circuit can be fired simultaneously in order that the circuitry detecting faults may be checked.

Note that in Figure 11 the current in L rises and falls sufficiently rapidly to prevent even a fairly small fuse from melting. Also, when $I_D$ stops, the stored energy in the inductors charges up C during which time the voltage across $S_1$ will rise at a few volts per microsecond until it becomes about 2E+300V.

## Fuses

No really adequate solution to the fusing problem exists. The leg fuses shown in Figure 3 present a problem. They are there to prevent major damage should the load short to ground and also they provide better protection for the SCRs in the event that the SCRs in <u>one</u> leg should be conducting simultaneously. (If all the SCRs fire simultaneously, it is the fuses in the $DC^+$ lead which protect the SCRs.) However, if the leg fuses fatigue during normal operation (and the others do not) then the stored energy in the load and in the current limiting inductor will cause the fuse voltage to be large which places a voltage stress on the semi-conductor elements in the system.

One can juggle the manufacturer's values of $I^2t$ ratings for the fuses and SCRs under various conditions. The net result is that, except at levels below four or five GeV, the fuses cannot protect the SCRs in the inverter. (They do protect the SCRs in the rectifiers quite well, however.)

It is proposed that we buy SCRs with two parallel semiconductor pellets. These SCRs will be very generously rated for normal operating conditions. In the event of a switching failure, they will also subvert one of the mechanisms of SCR failure; namely, the current in each pellet will rise to no higher than safe levels before the fuses will clear. However, the improvement in the $I^2t$ rating still will not be sufficient at 15 GeV to protect the SCRs should a failure occur which is not cleared by the fuse saver.

Max. allowed $I^2t$ for the present SCRs is about $2 \times 10^5$

Max. allowed $I^2t$ for SCRs with parallel pellets is about $3.6 \times 10^5$

(Both ratings given with consideration of the actual fault conditions anticipated.)

Fuses could be made which melt and extinguish more quickly than the present ones. However, their arc voltage will be much greater. For the main fuses, this is no disadvantage; for the leg fuses the added arc voltage might put an intolerable stress on the semiconductor elements.

$$\frac{(I^2t)\ \text{to clear}}{(I_{rating})^2} \doteq 0.6$$ for present fuses (lower for 10 GeV operation and below) (Type A50P or A50Z, Chase-Shawmut)

$$\frac{(I^2t)\ \text{to clear}}{(I_{rating})^2} \doteq 0.3$$ for fuses contemplated for replacement of present main fuses (Type A70P, Chase-Shawmut)

Bias Current Regulation

The bias current is controlled by regulating the sum of the voltage outputs of the six DC supplies around the ring with a fast voltage control loop. This is followed by a slow control loop which regulates the current.

There are five unregulated three phase full wave rectifiers (whose outputs are effectively in series) around the magnet ring. The input voltage to the transformer primaries of these supplies can be roughly set. An Inductrol serves to vary this voltage. In addition, there is a phased-back (SCR controlled) supply whose voltage can be varied rapidly. The voltage feed to the unregulated supplies is adjusted (either automatically or manually) such that the voltage of the regulated supply is in the mid-range for the desired current in the magnets. A small rectifier bridge samples the voltage feed to the unregulated supplies. Its output is called the simulacrum voltage. The voltage regulation loop "considers" the sum of some fraction of simulacrum voltage and the regulated supply voltage. The set-point voltage for the voltage loop is provided by both a signal proportional to the current set-point but also an error signal provided by the current regulation loop. The voltage loop has an open loop gain of from 10 to 30 depending on the region of operation. It is not useful to have a very much higher loop gain because the simulacrum voltage is not more accurate than 5% and because the magnet inductance allows the slower current loop to react before appreciable changes in the magnet current have occurred following a line voltage step. There are also problems associated with the variation of the voltage loop's phase response as the voltage loop's open loop gain varies with operating conditions. If the phase response varies too much it is hard to close the current loop stably.

The current loop measures the shunt voltage and compares this with the current set point. The shunt is placed at the output of the phased-back supply preceeding an LCR filter. At first sight this does not appear to be a favorable point. At very low frequencies the shunt current and the phased-back supply voltage are in phase. At about f = 1/10 Hz the magnet ring's inductance causes a phase lag of the shunt current. At about f = 1 Hz the magnets' inductance resonates with the capacitance of the filter. Above this frequency the shunt current leads the supply voltage. The attenuation caused by the resonance of the magnets' inductance with the filter capacitance with the favorable phase shift in the region of one to ten Hz is utilized. In addition, having the shunt directly at the output of the phased-back supply simplifies the problem of finding a suitable electrical common point for the electronics. (No electrical ground exists in the system.) The system is not without difficulties but the net result is a loop which when closed has useful loop gain at a frequency of about one cycle.

The original design of the current loop had two dominant time constants of about 10 seconds each. The system was stable under all conditions but exhibited unfavorable properties during the periods when the loop was effectively open because the amplifiers were not in their linear regions. Two equal delaying time constants constitutes a virtual delay in the system roughly equal to the time constants themselves. But because of the high loop gain, it is possible for the effective delay to be much longer. Thus, suppose that the loop is trying vainly to increase the current while the phased-back supply is full-up and the unregulated supplies are putting out insufficient voltage. Now, suppose that the voltage of the unregulated supplies is being increased as rapidly as possible. Suddenly, the current becomes sufficient. However, the delay in the loop cannot allow the phased-back supply to return to a normal voltage for some time. By that time the first amplifier in the loop may be saturated in the opposite direction from the original conditions while the second amplifier may not yet have called for a reduction in the voltage. The net result is that the system may take several time constants to settle down. Presently the system has one dominant time constant of about 100 seconds. Short term regulation is better than 0.05% of 10 GeV excitation.

Slope Regulation

The AC magnet current is regulated by maintaining the slope of the overall magnet ring current at injection time at some desired level. The AC magnet supply consists of voltage regulated DC supplies followed by LC filters and the inverters. The set point of the DC supplies is determined by comparing the observed slope with a desired slope setting. The voltage regulation loop in the DC supplies has an open loop gain of about 30. It may be that this loop should have a higher gain. The problems encountered in stabilizing the slope regulation loop are formidable:

1. The LC filter following the DC supplies has very nasty properties. It cannot be modified to have more gently varying phase and amplitude variations as the LCR filter in the bias current regulation loop has been.

2. The filling time of the magnets is not a clean cut, nor readily measurable, quantity.

3. Without the inclusion of non-linear elements, the open loop gain of the slope control loop would be proportional to peak energy. Such a non-linear circuit is used.

4. The slope loop's open loop gain is approximately proportional to the reciprocal of the slope. Fortunately, at higher slopes, the slope loop response time is less critical. The loop is optimized for slopes corresponding to $\frac{1}{2}$ MeV/turn and is stable as low as $\frac{1}{5}$ MeV/turn.

5. Closing of the slope control loop depends upon the existence of a slope reading.

It is impossible to have a slope reading until the AC current in the magnets is approximately equal to the DC current. Providing for a smooth transition from open loop conditions to closed loop operations upon turn-on is a major design problem. A small signal, corresponding to a slope of about 0.1 MeV/turn is provided when there is no real slope signal (to provide smooth turn on).

Originally, the slope control loop had two dominant time constants each of the order of ten seconds. The result of changing to one time constant was similar, but more dramatic, to that encountered with the bias current control loop. Upon turn-on the inverter supply voltage rises until a slope signal is available. At this point, the loop may or may not be open because of saturated amplifiers. Even if the loop closes at this point, the virtual delay (with two time constants) caused the supply to continue to rise for some time. What happened then is that when the control started to "catch", the loop was driven back so far that the AC current is reduced to the point where no slope signal was available. The inverter does not take kindly to rapid variations of the supply voltage and the system often faulted. The solution was to convert to one very long time constant. Upon turn-on, this time constant is discharged and no inverter supply voltage is demanded. By controlling <u>not only the time constant</u>, but also the maximum rate at which it could be charged, one can control the rate of rise of the supply voltage such that the control loop is always in the linear region so that the moment that a slope signal appears the loop will close (stably) and the effective time constant of the loop will be the dominant time constant divided by the open loop gain.

The slope loop has useful gain at about one Hz. However, many problems still are to be faced. Of these, a better signal representing the slope at injection is the most obvious. Presently, the slope signal is derived by sampling (for 8 microseconds) the voltage on a pick-up coil in the test magnet. This voltage is plagued with "little men" which cause the slope reading to vary from the true value. It is proposed to read, instead, the time between the peaking strip pulses divided by the DC current set-point voltage. A lucky accident allows this quantity to be read easily and also it is fairly accurately proportional to the slope.

Another major difficulty with the AC magnet power control - one which is not unique to it - is that the timing of the inverter and of the rectifiers is determined by zero-crossings of the line voltages. Gross line variations upset these timings considerably. For instance, the inverter timing comes from a power line signal supplying the RF modulation, when the RF crowbars it will very likely trip out the inverter because of a timing error. In addition, there is evidence that the rectifiers for the AC talk to the DC supplies through the lines. Some effort has been made to stop this by placing capacitors to ground on each of the incoming phases to the regulated supply for the DC magnet power. It <u>is</u> known that without these it will not work when other large equipment is working.

SCR Gate Drives

For large SCRs one can consider the gate as extended over a large perimeter. Not all sections of the gate may require the same gate voltage drive. One way to insure that the entire gate is activated at one time is to have the gate drive signal be large in voltage. In addition, the gate, when triggered, activates only a small fractional area of the semiconductor pellet immediately. Activation of the pellet takes about 25 microseconds with a healthy gate drive. Hence, the dI/dt rating of the SCR is partly determined by the rate at which the area is activated and the peak allowed current for the SCR. For the 840 Amp pellets, one would conclude from this mechanism that dI/dt might be of the order of 10,000 Amps/25 microseconds. For these larger SCRs, the manufacturers are very coy about saying directly that higher dI/dt ratings than 50A/μsec are allowed, but they do suggest that they are.

Another turn-on property which must be considered is the instantaneous power per unit area within the junction during the time that the voltage across the SCR drops from the initial large forward voltage to some small voltage (say 10 Volts) during turn-on. If, for example, the voltage takes 4 microseconds to drop (linearly) to a negligible voltage and the dI/dt is 50 Amps per microsecond while the initial forward blocking voltage is 600 Volts, then the maximum instantaneous power would be 60,000 Watts which is about the instantaneous maximum power rating for the entire pellet. (It is interesting to note that at a given initial forward blocking voltage, almost all SCRs have the same dI/dt rating.) Obviously, that section which carries the initial current of the pellet heats very rapidly. It has been observed that the harder one drives the gate, the faster the voltage across the SCR drops. A gate rise time of one microsecond is obviously not conservative.

G.E. is now suggesting that gate rise times of the order of one Ampere in 100 nanoseconds are required. In the light of this statement, the following recommendations are made:

1. Rectifier SCRs. The present transformers are somewhat better constructed than those for the inverters. The rise time of the gate is probably sufficient. However, the 100 nF capacitors in parallel with the gate should be reduced to 20 nF or so. The present drive has a short circuit current of about two amperes and an open circuit voltage of about 10 Volts which is within the original gate ratings. The pulse length must be at least 150 μsec.

2. Inverter SCRs. The present transformers step-down the 24V pulse voltage to 16 Volts. It is not clear what the gate drive specifications on the present (C500X1) SCRs are. The original specifications given to me were the same as for the 470 Ampere SCRs but the specifications for the C501 series are for 16 Volts peak gate drive rather than 10 Volts. The recommended load line for the C501 is for 25V open circuit voltage and about 2 Amps short circuit current. For the present SCRs with the low rate of rise of the current (dI/dt ± 10A/microsec at 10 GeV), it should be sufficient to modify the gate drive by using a 1:1 transformer and changing the feedline to the transformer from shielded-twisted pair to coax. It definitely does appear that the shielded-twisted pair limits the rate of rise of the current considerably. The voltage measured on the transformer primary has a poor rise time while the voltage on the rectifier trigger transformers rises sharply (at the end of a coax of considerably longer length than the shielded-twisted pair). We have shown that, on the bench it is possible to achieve a rise time (into a 7 ohm resistive load) of about one-fourth microsecond/Amp on the secondary of the transformer and with 100 feet of coaxial cable between the transformer and the driving transistor.

One of the gate transformers has been replaced in an inverter. It has 15 turns on each winding. The windings are interleaved. It would be sufficient to have 14 turns or even 12 (the number easily wound on the core in a single layer). The pulse length must be 40 microseconds or longer.

If the C501G1 SCRs are purchased (with parallel pellets) the drive may have to be upgraded to assure that both pellets will fire simultaneously so that both will conduct later in the cycle.

3. Crowbar SCRs. The triggers to the crowbar SCRs are critical because the crowbar will experience a large value of dI/dt upon firing into a fault (dI/dt ≐ 50 A/microsecond) and an even larger value (perhaps twice as high in the event the crowbar should fire without a fault). (The SCRs can handle higher value of dI/dt when operated on an intermittent basis and/or when the pellet is cool.) In addition, a false crowbar firing is done while the voltage across the crowbar SCR is large. Some effort should be made to insure good triggering for the crowbar SCR. It may be necessary to use a SUS or other more complicated circuitry to achieve a fast enough gate drive. We plan to use the 1800V C500's indefinitely for this purpose.

Extension to 15 GeV

There are many problems associated with extension to 15 GeV. Some of them can easily be solved for 14 GeV operation while others, such as fusing, remain intractable. A short list of the important parameters to be considered in such an extension is given below:

1. Different values of L, C, and R will be required in the crowbar.

2. More study of fusing.

3. A study of what will happen to the traveling waves caused by the harmonic content of the DC supplies around the ring when some are run directly off the line and others are fed from the Inductrol.

4. Whether the regulated DC supply is rated for 320 Amps at all output voltages.

5. The power and current required to run the machine (at any particular energy) is significantly higher than anticipated as are the line drops in the incoming power lines.

6. How to handle the mistuning of the magnet ring as the temperature increases in such a way that it will be possible to get to 15 GeV with the AC power supply and the change of phase of the quadrature components of the power supply ripple as the tuning changes.

# FOOT NOTES

*Work supported by National Science Foundation

1) M. G. White, F. C. Shoemaker, G. K. O'Neill, A High Intensity Proton Synchrotron, CERN Symposium Bd1, H150, S525 (1956).

2) R. R. Ott, L. A. Schlabach, A Unique Silicon Controlled High-Power Inverter with Sine-Wave Output Voltage. Digest of Technical Papers, 1962 International Solid State Circuits Conference (IRE, AIEE), p. 100. We became aware of this paper after development of our 20kW prototype. They suggest more complicated commutation filters which are desirable when load voltages must be maintained constant while the load impedance varies in phase and magnitude.

3) The SCRs used in the inverter are General Electric C500X1's. They consist of two 840A, 1800V units mounted back to back for use in AC switching. The integral water-cooled heat sink is very attractive. For sinusoidal output from the inverter we are using these SCRs for conduction in one direction only.

4) G.E., SCR Manual, 4th Edition 1967.

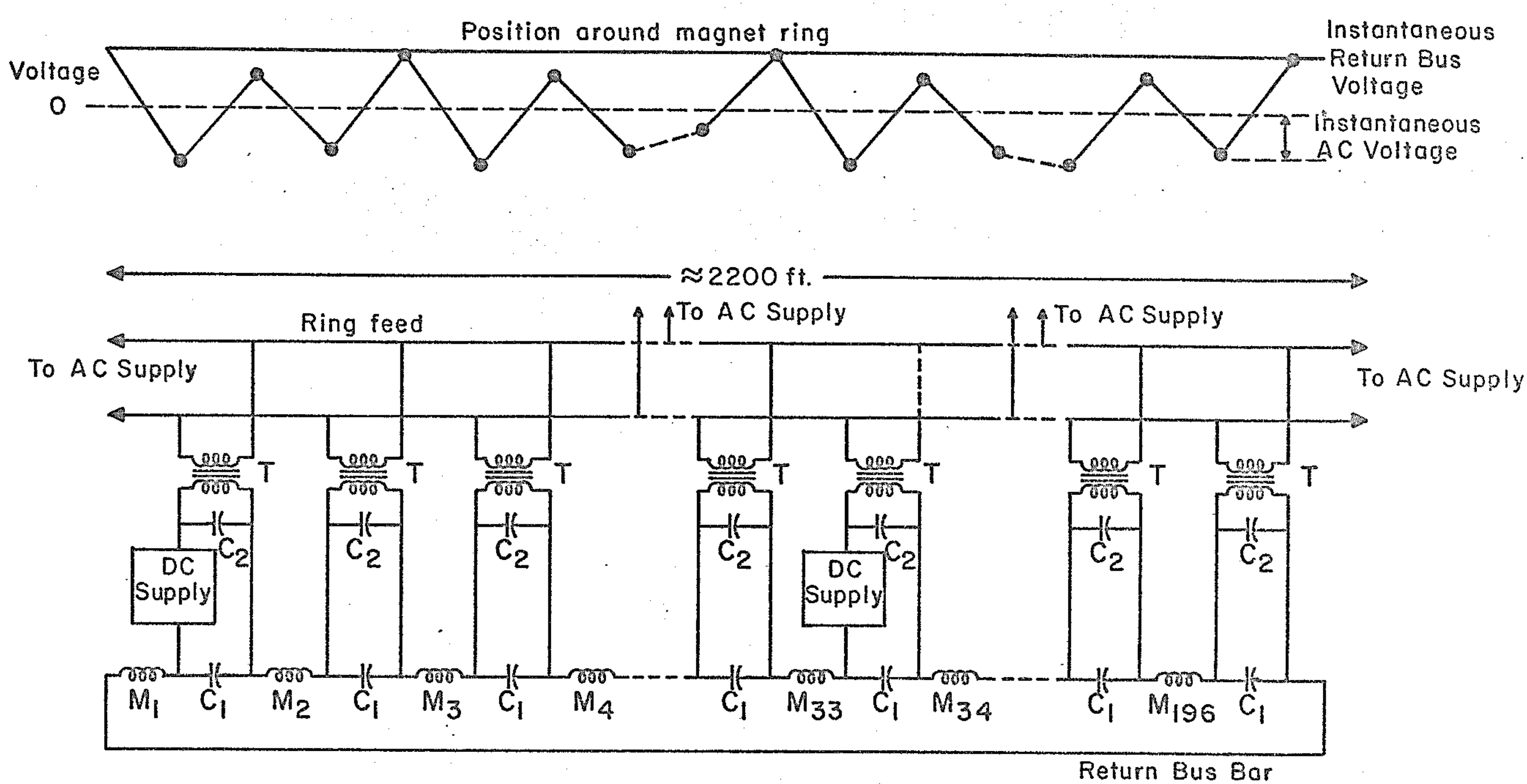



FIGURE 1 SIMPLIFIED DIAGRAM OF MAGNET INTERCONNECTIONS

6 DC SUPPLIES. ONE EVERY 32 OR 33 MAGNETS.

$C_1$ AND $C_2$ ARE JOINED AS SINGLE BANKS OF CAPACITORS EXCEPT AT SIX POSITIONS OF DC SUPPLIES. THEY ARE ADJUSTABLE IN 10μfd STEPS

$C_1 \approx C_2 \approx 950\mu fds.$

FEED FROM AC SUPPLY IS CONNECTED TO "RING" FEED AT THREE POINTS AROUND THE RING.

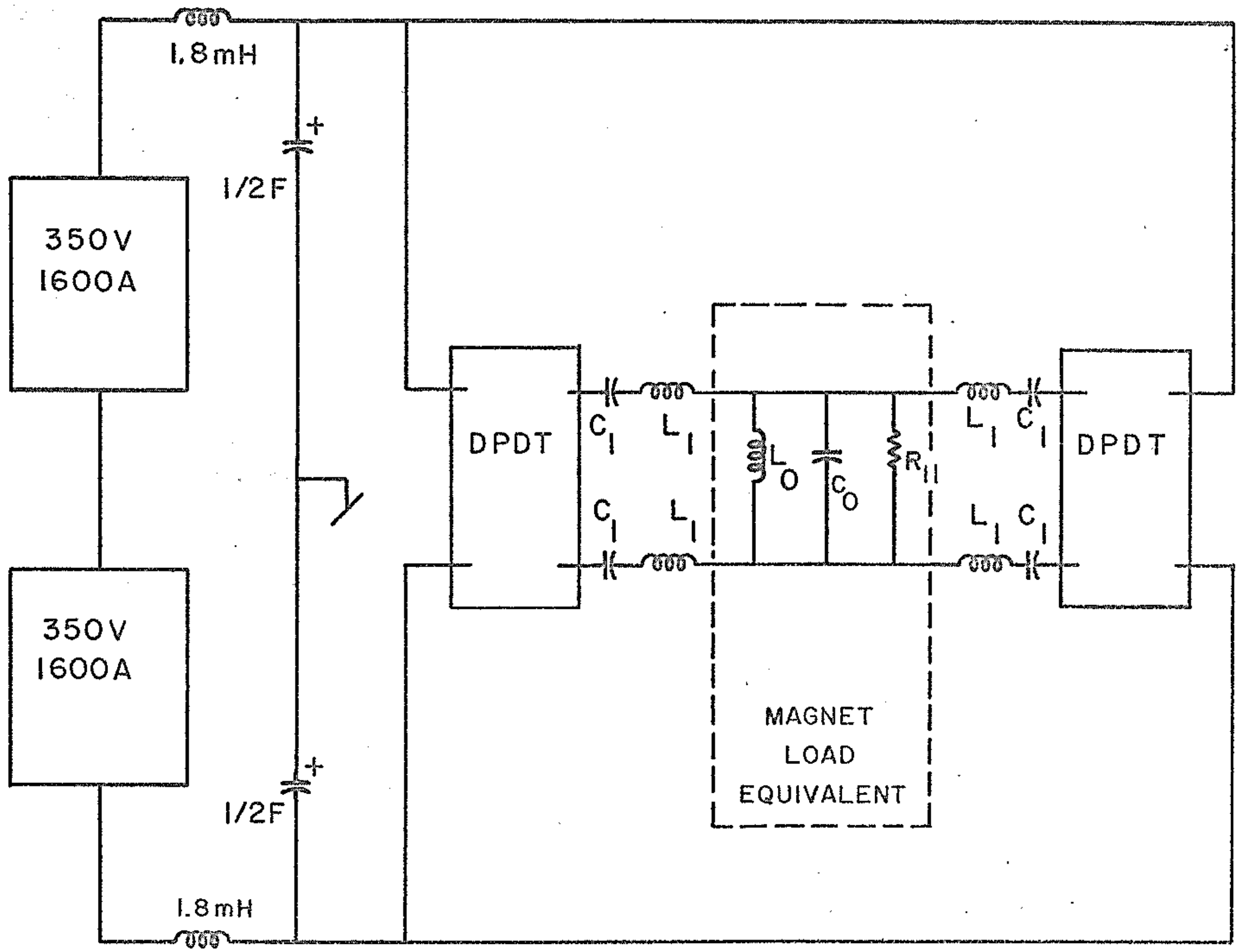



FIGURE 2 INVERTER BLOCK DIAGRAM

$$\omega L_1 \approx 0.5\Omega, \frac{1}{\omega C_1} \approx 0.9\Omega, R_{11} \doteq 0.4\Omega = 60\omega L_0 \doteq 60/\omega C_0, f \doteq 60H_Z$$

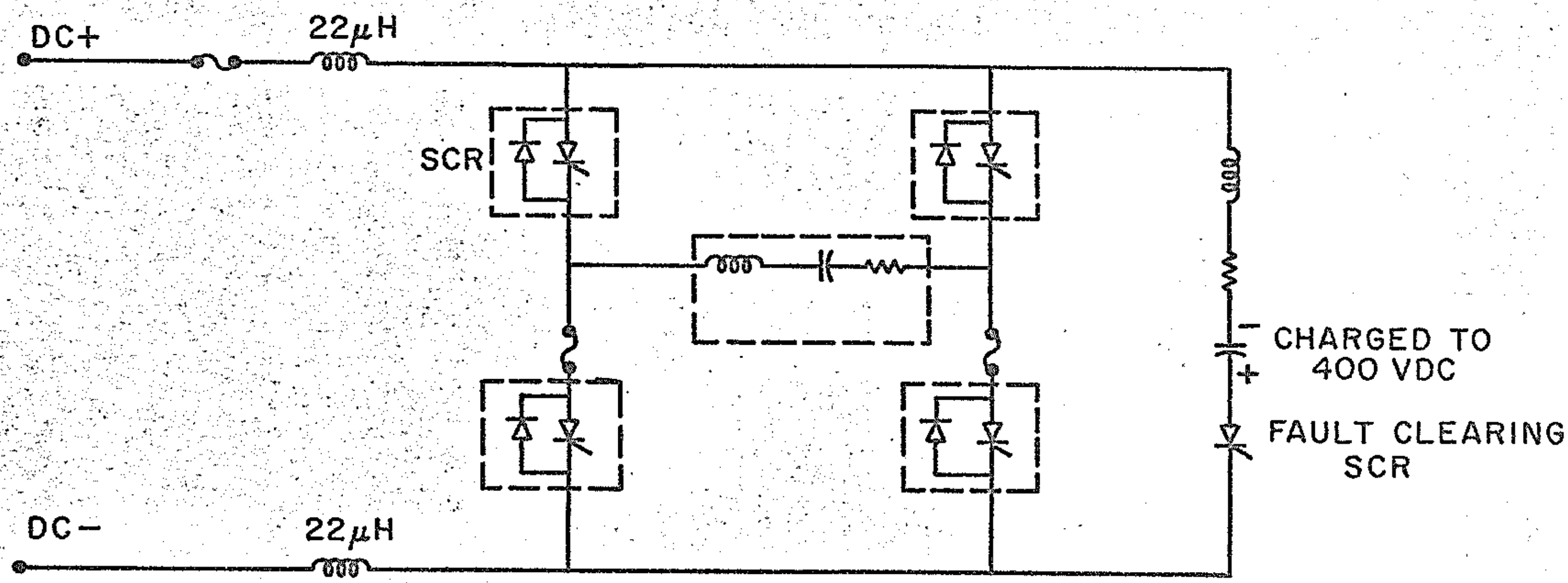



FIGURE 3 INVERTER SCHEMATIC

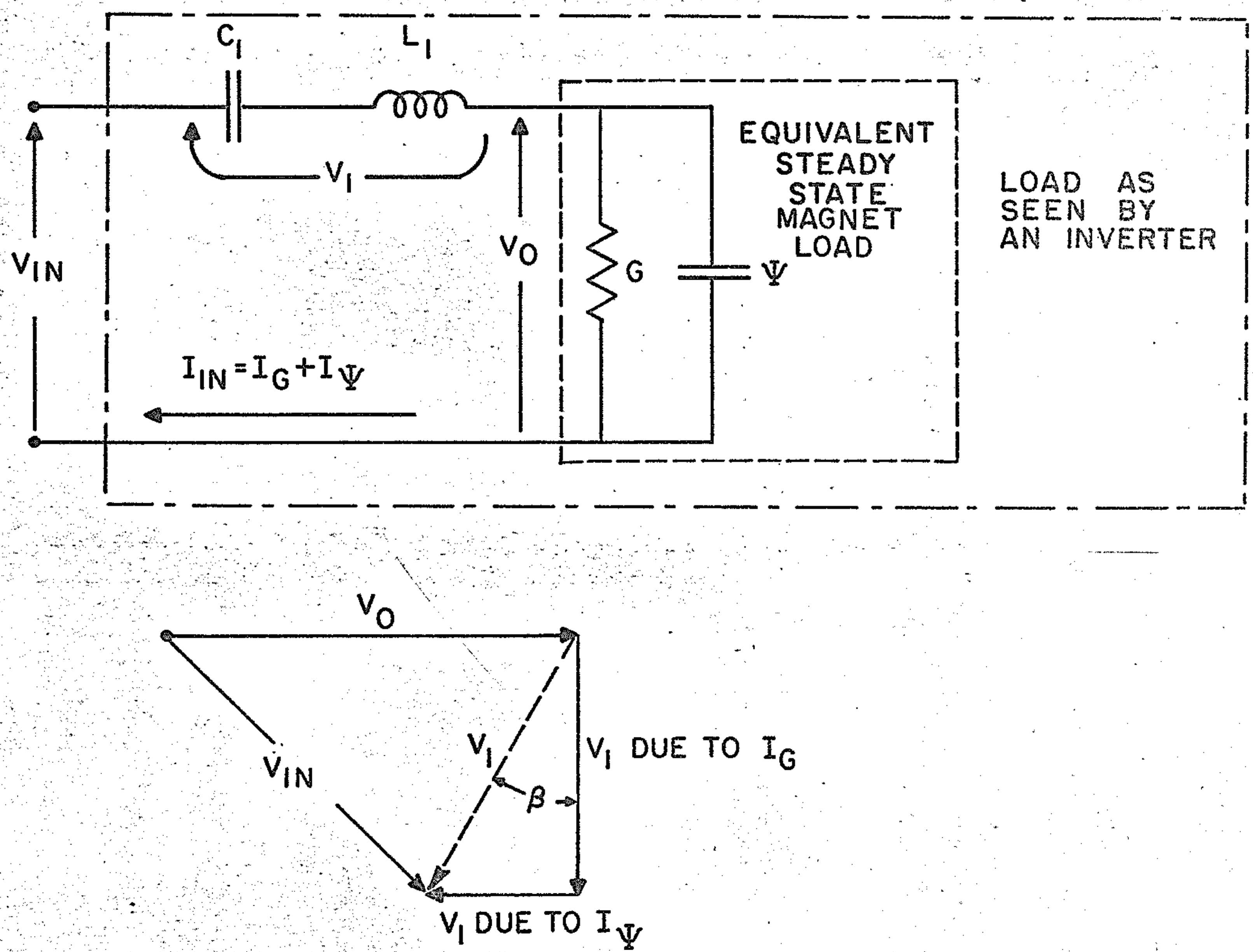



FIGURE 4 EQUIVALENT CIRCUIT FOR STEADY STATE ANALYSIS

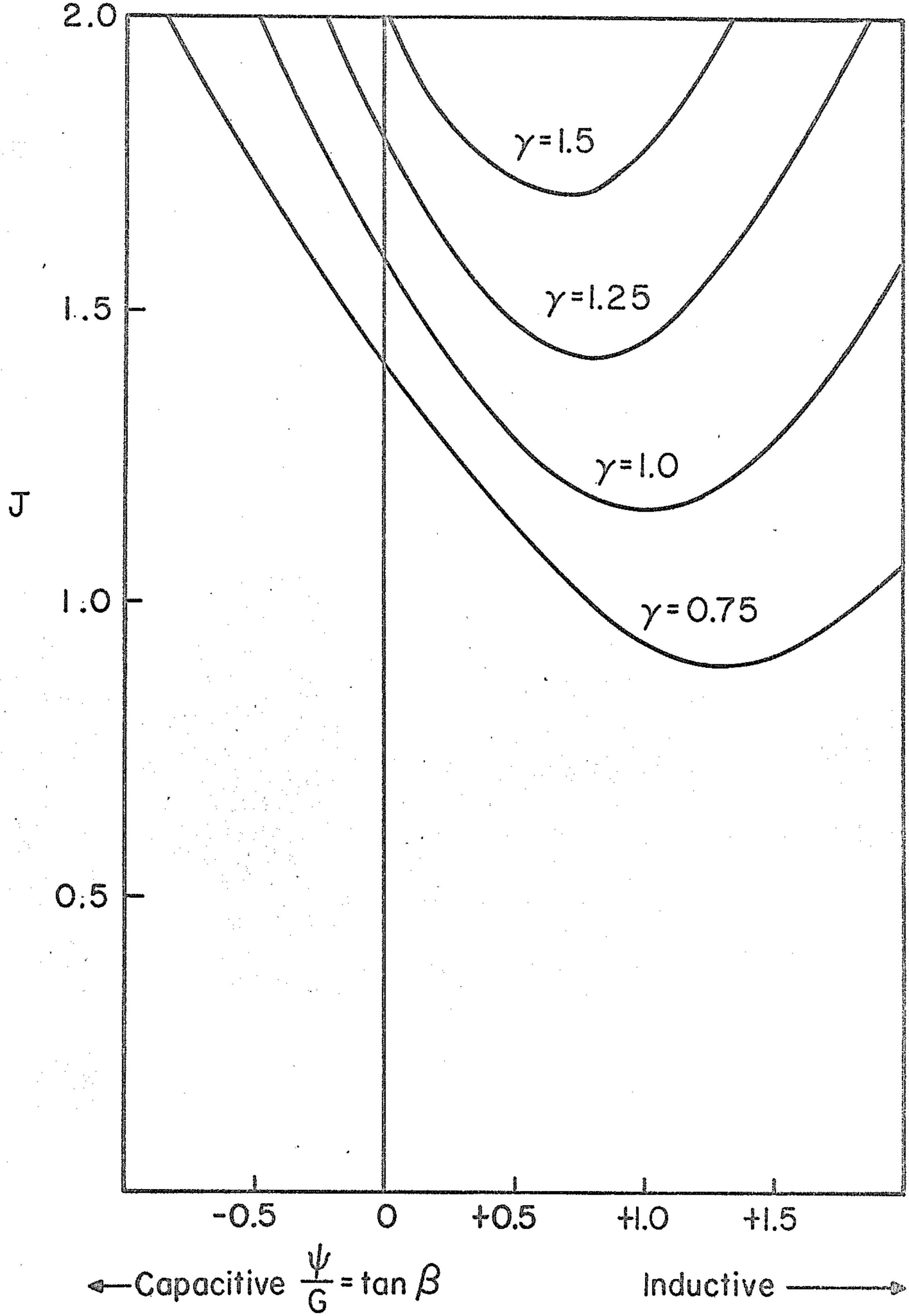



FIGURE 5 RATIO OF INPUT DC VOLTAGE TO AC LOAD VOLTAGE, J, VS. TANGENT OF PHASE ANGLE OF MAGNET LOAD.

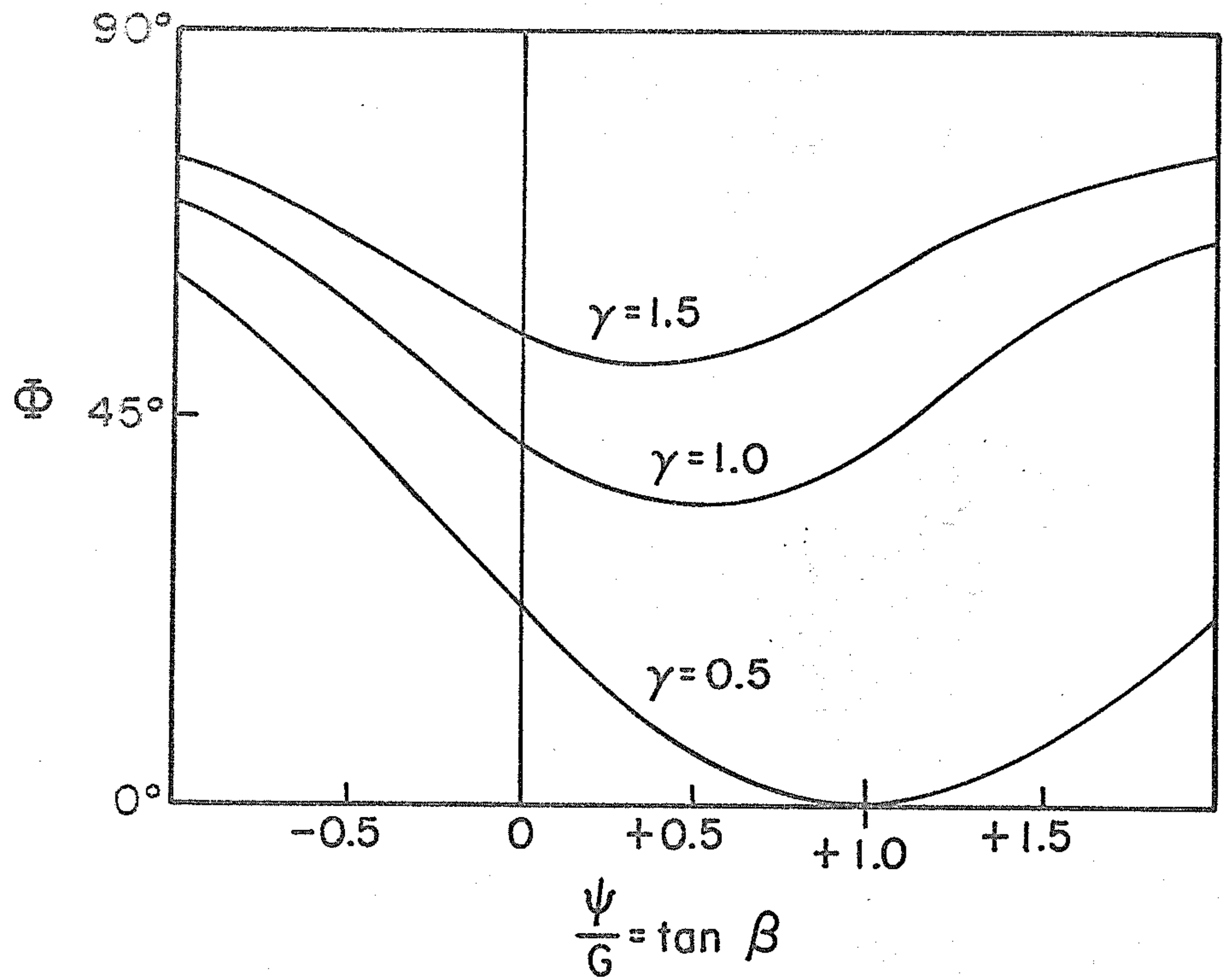



FIGURE 6 CONDUCTION ANGLE OF REVERSE DIODES VS TANGENT OF PHASE ANGLE OF MAGNET LOAD

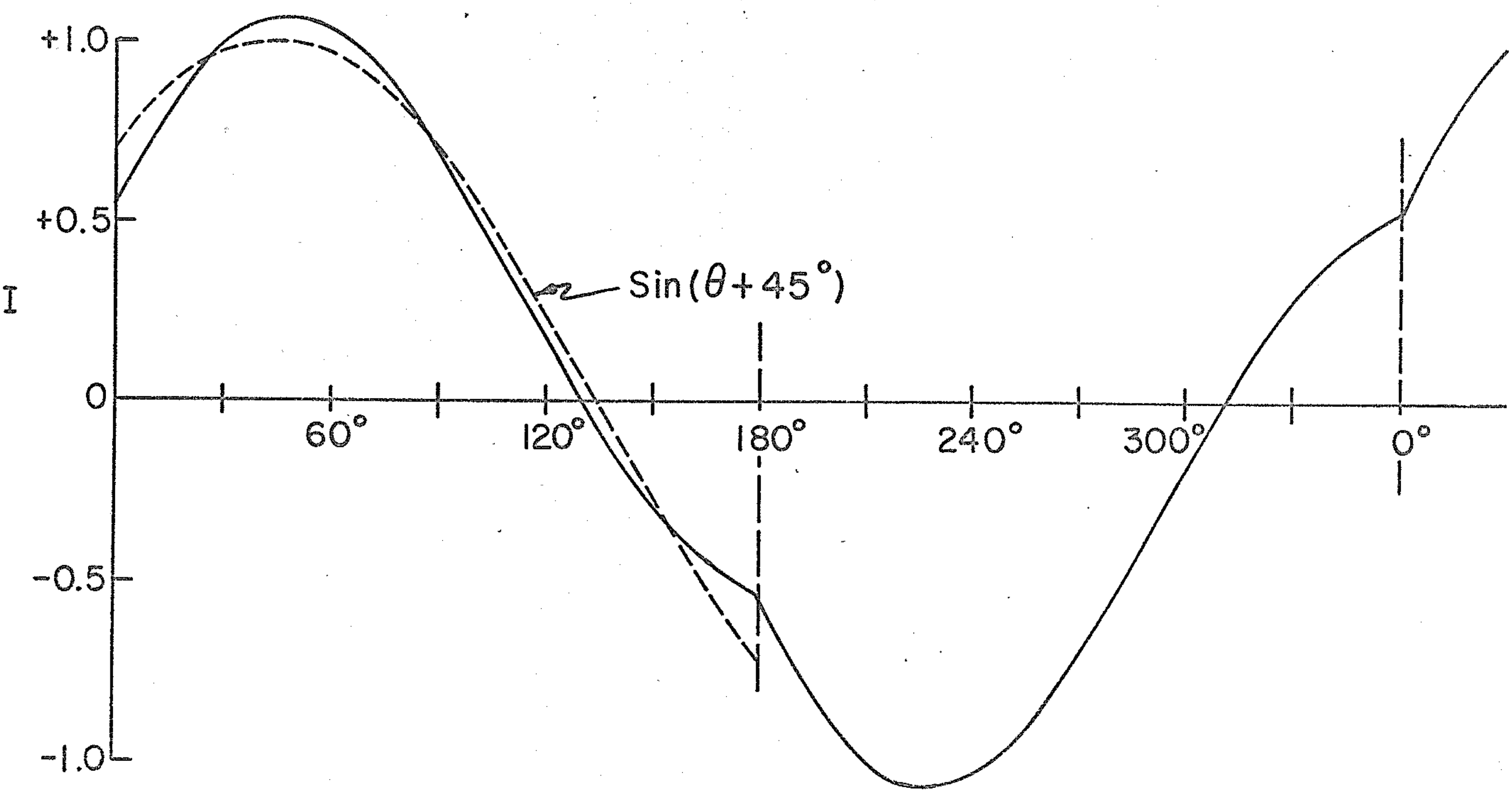



FIGURE 7 INVERTER OUTPUT CURRENT VS TIME

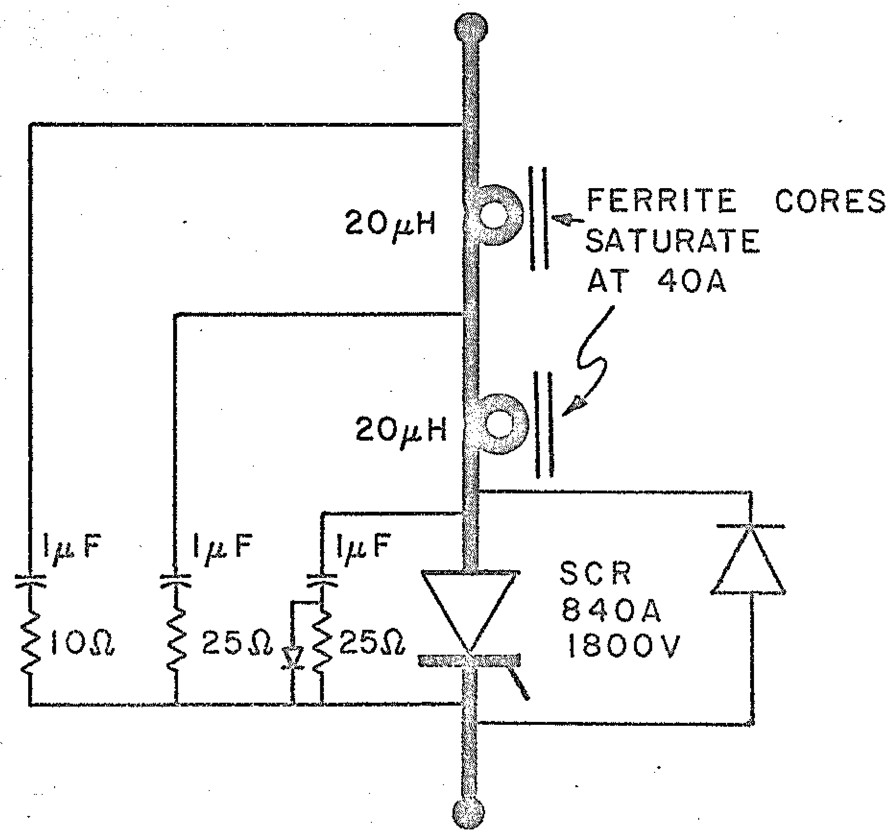



FIGURE 8 SCR MODULE

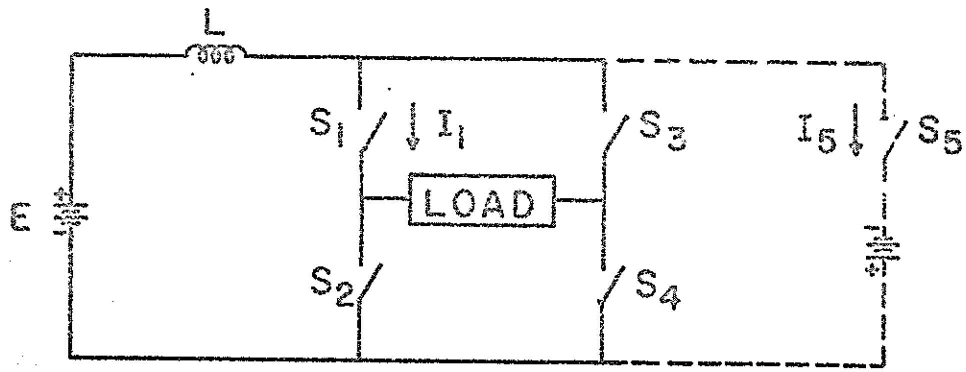



FIGURE 9 SIMPLIFIED INVERTER SCHEMATIC

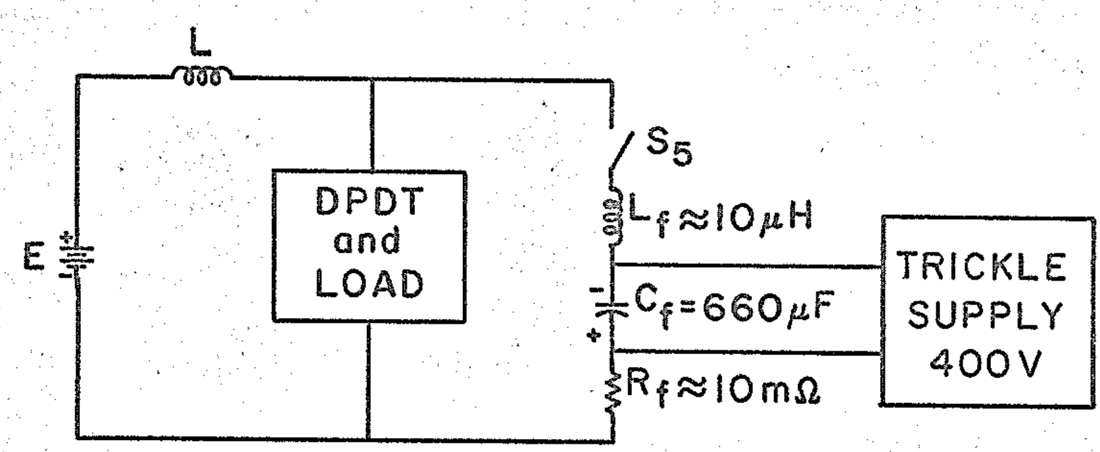



FIGURE 10 CRAWBAR BLOCK DIAGRAM

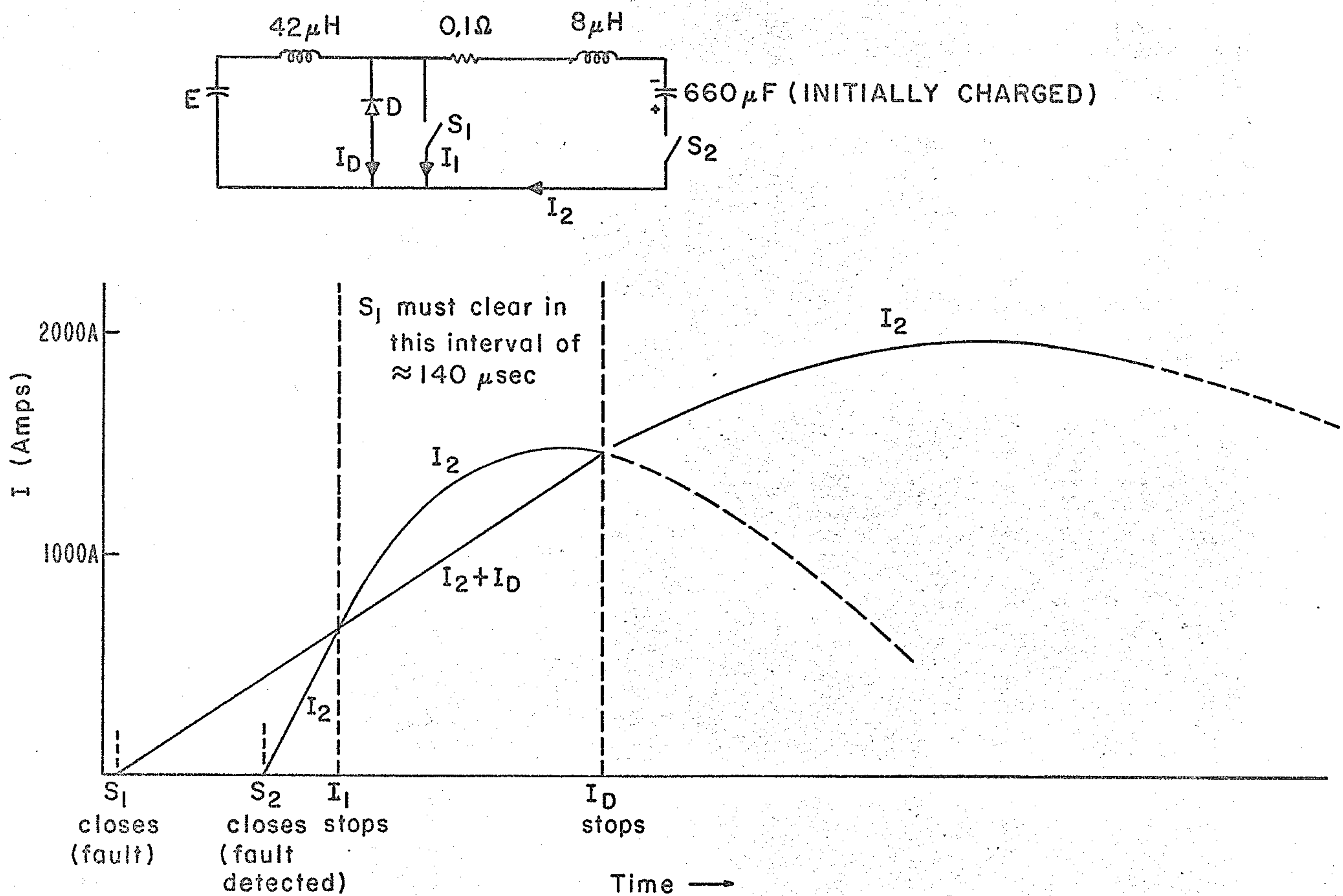
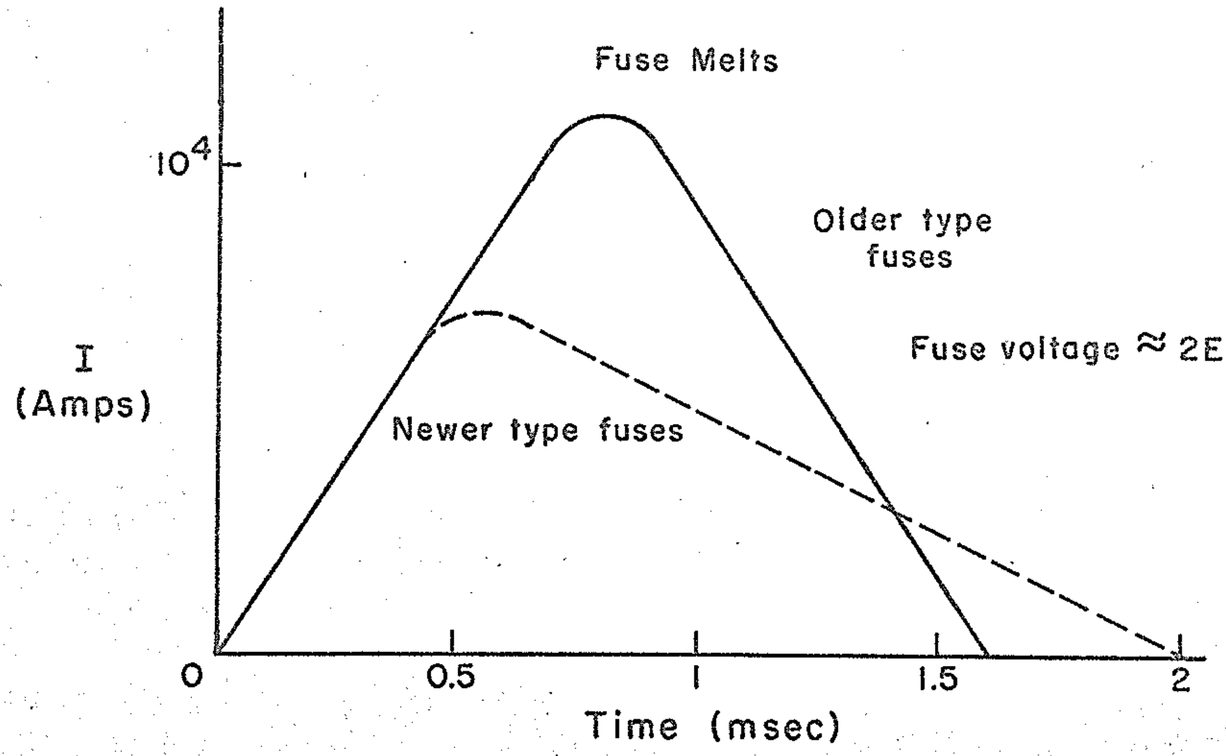
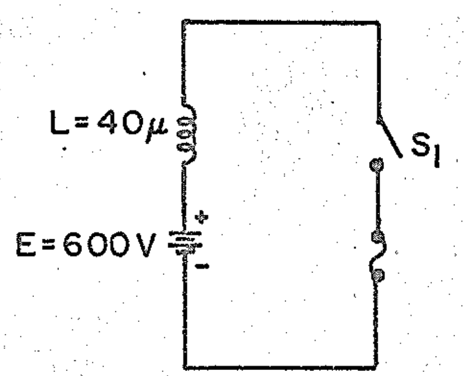



FIGURE 11 INVERTER CURRENTS DURING CROWBAR OPERATION




$$\left(\int_0^{\text{cleared}} I^2 dt\right)_{\substack{\text{Older}\\ \text{Type}}} \Big/ (I_{\text{rating}})^2 \approx 1$$

$$\left(\int_0^{\text{cleared}} I^2 dt\right)_{\substack{\text{Newer}\\ \text{Type}}} \Big/ (I_{\text{rating}})^2 \approx 0.3$$

FIGURE 12 FUSE CURRENT DURING CATASTROPHIC FAILURE (IDEALIZED BUT NOT A BAD APPROXIMATION)

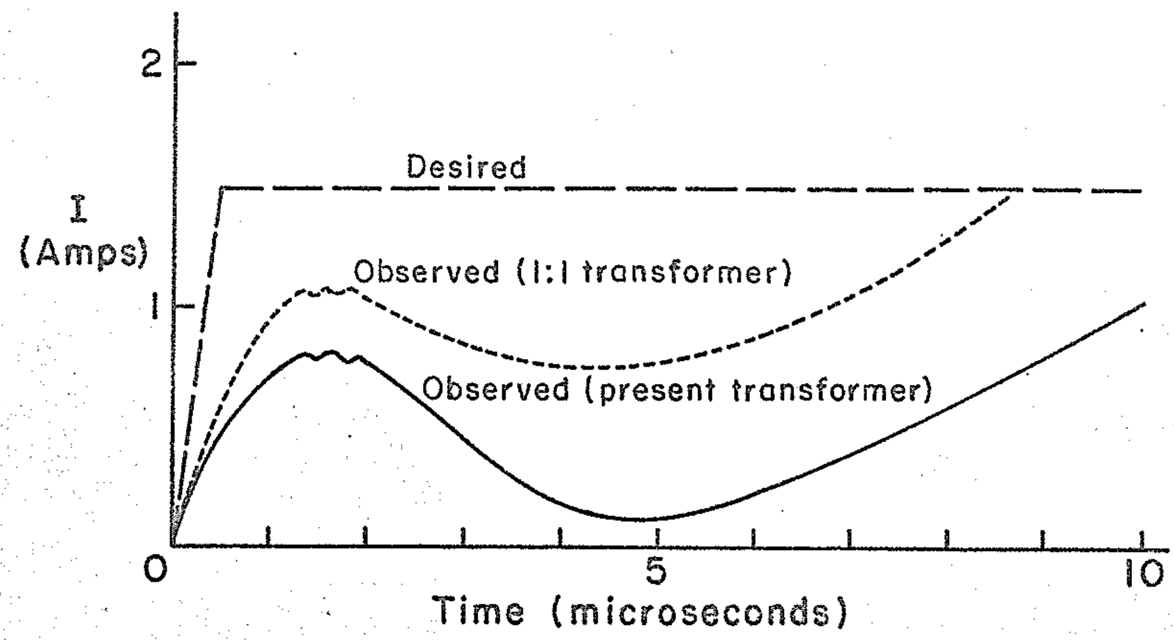



FIGURE 13 SCR GATE DRIVE FOR INVERTERS