CS-38

A 44 CHANNEL DIGITAL VOLTMETER

Laboratory of Nuclear Studies

Cornell University

Wayne Rial

2 January 1968

44 Channel Multiplexing Digital Voltmeter

A multi-channel, multiplexed, digital voltmeter with 4 place accuracy was required for monitoring various DC control voltages throughout the Cornell 10 GeV synchrotron. Since no commercial unit was available that would perform the required functions, we decided to design and construct a custom built DVM to measure the desired parameters.

Basic Philosophy:

A linear, 4000 step staircase is generated by standard D-A techniques using BCD coded 8-4-2-1 binaries and a precision, weighted, resistive-ladder network. The generated staircase-waveform is fed to one input of a differential comparator and the unknown voltage to be measured fed to the other input of the same comparator. When a coincidence in voltage appears between the unknown voltage and the corresponding voltage step of the staircase, the comparator triggers a flip-flop, initiating a readout cycle. During the readout cycle, the number of steps in the staircase to that comparison level is determined, and the number of such staircase steps is subsequently displayed on Nixie readouts. During the readout cycle, the progression of the staircase-waveform ceases and later continues advancing upon completion of the readout cycle. The staircase thus continues advancing until another (higher) unknown voltage coincides with another particular step on the staircase waveform, triggering another differential comparator, initiating a new readout cycle, and displaying that staircase-step number on a different group of

Nixie readouts. Each comparator has a particular bank of Nixie readouts associated with it.

Upon completion of 4000 staircase steps and their appropriate readout cycles, the staircase to waveform is returned to zero, and after a special delay period, commences a new measuring cycle.

The basic scheme thus far appears in Fig. #1.

Physical Description of Instrument:

The 44 channel DVM is completely self-contained except for the unknown voltage input-lines and the remote Nixie-indicator banks. The unit proper contains all the logic, made up of some 50 logic cards, power supplies, three local Nixie banks, and auxiliary switches and controls.

The instrument is divided into sections whose functions are, from top-to-bottom,

top panel - local Nixie readouts
2nd " - blank panel for later additions
3rd " - card file containing 22 input-comparators
4th " - input voltage switches and controls
5th " - card file containing 22 input-comparators
6th " - miscellaneous controls
7th " - card file containing logic, and
" " " logic and Bipco gates
8th " - output switches and remote Bipco connectors
9th " - main power supply

The second through eighth panel sections are mechanically tied together and constructed as a integral unit. These sections should be maintained as a unit to minimize ground loops.

The system employs some 2317 transistors, 2090 diodes, with a total component quantity of about 9000.

There are three Nixie banks of four digits each in the rack (top panel). The left-hand bank displays the reference-voltage step in the staircase waveform which occurs at the 2000th staircase step (exactly in the center of 4000 step staircase) and normally displays the number 2000 during DVM operation. During initial equipment warm-up, the left-hand Nixie bank hunts from 4000 to 0000, settling down to some arbitrary number and thence counting towards the reference-voltage step, eventually arriving at number 2000. Occasionally during normal operation, the reference-voltage Nixies will momentarily jump to numbers 1999 or 2001 while reference-voltage drift is being corrected to correspond to the number 2000.

The central Nixie-bank can display the equivalent input voltage to any voltage-comparator by means of selector switches located on the fourth panel. Thus, the actual input-voltage to any comparator can be monitored locally.

The right-hand bank of Nixies can dispaly locally, the number that any one of the remote Nixie-banks is displaying, by means of selector switches located on the ninth panel. Thus, the measured input-voltage to any comparator can be locally displayed.

The desired readouts (Nixie-banks) are generally located remotely to the main instrument. Provisions have been made for the remote readouts to be placed up to 100 feet (of interconnecting cable) from the instruments. The DVM has been designed so that approximately 12 banks of 3-digit readouts, and 30 banks of 4-digit readouts can be used remotely.

The number of digits per readout can be changed by utilizing different Nixie-driver gates or constructing new gate cards. Thus, it is possible to have all of the 44 Nixie-banks displaying 4 digit accuracy.

The remotely-located Nixies will usually be located on a panel associated with the control which varies the DVM input voltage to be measured. This control may be a manually-operated potentiometer or a motor-driven potentiometer operated by slewing switches or computer control. A remote Nixie-bank may also, of course, indicate the voltage measured across a sampling resistor not associated with a manual control.

Electrical Characteristics of the Instrument:

The input voltages to be measured by this instrument are negative D.C. values with respect to system ground (input reference) with a maximum of -10 V amplitude. The system can follow a rate-of-change of input voltage $(\frac{de}{dt})$ not greater than about 50 volts per second, although such input rates-of-change can not be followed visually on their respective Nixie readouts.

The transistors in the comparator input circuit are protected against overvoltage of the input lines so that accidental application of excessive positive or negative voltage will not incapacitate the instrument.

Instrument Logic:

In the description of the logic, all functions are considered true when the waveform goes to a positive value. The actual circuit waveforms may or may not be true for positive going values. The logic utilized in the instrument uses both positive and negative

logic and care must be exercised when deciphering the logic sequence. The timing-chart shows the true-false relations of the various switching functions, and the respective timing-chart waveforms are not to be construed as the actual logic waveforms.

In studying the logic, reference must be made to the timing chart, block diagram, and the following definitions.

Logic Definitions

$\overline{|Q}$ = leading edge of Q function

$\overline{|\bar{Q}}$ = leading edge of $\bar{Q}$ function

$\overline{Q|}$ = trailing edge of Q function

$\overline{\bar{Q}|}$ = trailing edge of $\bar{Q}$ function

$M \longrightarrow N$ means a transition of M causes N to go true

$M \longrightarrow \bar{N}$ means a transition of M causes N to go false

G = H means G produces H (true)

		Location	
1.	CFF = comparator flip-flop	comparator	card
2.	RFF = readout flip-flop	clock	"
3.	DFF = main delay flip-flop	clock	"
4.	A Gate = A Gate output pulses (UCP)	clock	"
5.	B Gate = B Gate output pulses (DCP)	clock	"
6.	C = clock pulse	clock	"
7.	XFF = special delay flip-flop	clock	"
8.	YFF = special delay flip-flop	clock	"
9.	SFF = strobe flip-flop	strobe	"
10.	PDC = pause delay flip-flop	strobe	"
11.	JAM = jam pulse	strobe	"
12.	UCP = up count pulses	clock	"
13.	DCP = down count pulses	clock	"

14.	LP-30 = Commercial D to A converter	LP-30 card
15.	OA-30 = Commercial operational amplifier	OA-30 "
16.	FZ_1 = first zero flip-flop for 1's digits	Fst& Snd zero card
17.	FZ_{10}= first zero flip-flop for 10's digits	" " " "
18.	FZ_{100}=first zero flip-flop for 100's digits	" " " "
19.	FZ_k = first zero flip-flop for k's digits	" " " "
20.	SZ_1 = second zero flip-flop for 1's digits	" " " "
21.	SZ_{10}= second zero flip-flop for 10's digits	" " " "
22.	SZ_{100}=second zero flip-flop for 100's digits	" " " "
23.	SZ_k = second zero flip-flop for k's digits	" " " "
24.	SZ OR = OR'ed output of second zero flip-flops	down count pulse gates card
25.	PFF = pause flip-flop	up-down counter#4 card
26.	SZD_1= delayed second zero flip-flop for 1's	snd zero delay card
27.	SZD_{10}=delayed second zero flip-flop for 10's	" " " "
28.	SZD_{100}=delayed second zero flip-flop for 100's	" " " "
29.	SZD_k = delayed second zero flip-flop for k's	" " " "
30.	CLC = comparator latch circuit	comparator card
31.	K = 2000th staircase step binary output	up-down counter#4 card
32.	Ref CFF = reference flip-flop	reference comparator card
33.	STR = strobe pulse (ungated)	strobe card
34.	TPC = ten pulse counter output	10 pulse detector
35.	ZFF = special delay flip-flop	10 volt reference card
36.		
37.	C Gate = C Gate	down count pulse gates card
38.	D Gate = D Gate	" " " " "
39.	E Gate = E Gate	" " " " "

40. F Gate = F Gate down count pulse gates card
41. 4KC = 4000 count FF output
42. CFF_R = reference comparator FF

Logic Equations

1. $\overline{\overline{CLC_N}} \rightarrow CFF_N$
2. $\overline{\overline{CFF_N}} \rightarrow RFF, DFF$
3. $\overline{\overline{DFF} \cdot \overline{C}} \rightarrow XFF$
4. $\overline{\overline{XFF}} \rightarrow YFF$
5. $\overline{RFF} \cdot \overline{PDC} \cdot C$ = A Gate pulses (UCP)
6. $RFF \cdot \overline{DFF} \cdot C$ = B Gate pulses (DCP)
7. $\overline{\overline{DFF} \cdot \overline{C}} \rightarrow SFF$
8. $\overline{\overline{YFF}} \rightarrow \overline{DFF}$
9. $\overline{\overline{SZ\ OR} + \overline{4KC}} \rightarrow \overline{RFF}, \overline{XFF}, \overline{CFF}$
10. $\overline{\overline{4KC}} \rightarrow PFF$
11. $\overline{\overline{SZ\ OR}} \rightarrow \overline{PFF}$
12. $\overline{\overline{PFF}} \cdot STR \rightarrow PDC$
13. $\overline{\overline{PFF}} \cdot STR \rightarrow \overline{PDC}$
14. $SFF \cdot STR$ = staircase strobe pulses
15. First "0" from 1's down counter $\rightarrow FZ_1$
16. Second "0" from 1's down counter $\rightarrow \overline{FZ_1}$
17. $\overline{\overline{FZ_1}} \rightarrow SZ_1$
18. $\overline{\overline{SZ_1} \cdot \overline{C}} \rightarrow SZD_1$
19. B Gate $\cdot \overline{SZD_1}$ = C Gate pulses
20. etc. for $\overline{FZ_{10}}$, SZ_{10}, $\overline{SZD_{10}}$, = D Gate pulses

21. Etc. for FZ_{100}, SZ_{100}, SZD_{100}, = E Gate pulses

22. Etc. for FZ_K, SZ_K, SZD_K, = F Gate pulses

23. $\overline{DFF} \rightarrow \overline{FZ_1}$, $\overline{FZ_{10}}$, $\overline{FZ_{100}}$, $\overline{FZ_K}$, $\overline{SZ_1}$, $\overline{SZ_{10}}$, $\overline{SZ_{100}}$, $\overline{SZ_K}$

24. $\overline{SFF} \rightarrow JAM_1$ Reset all Bipcos

25. $\overline{PDC} \rightarrow \overline{CLC_N}$

26. $\overline{K} \rightarrow ZFF$

27. $\overline{K} \cdot \overline{UCP} \rightarrow \overline{ZFF}$

28. $\overline{K} \cdot CFF \cdot \overline{ZFF}$ = pump staircase

29. $CFF_1 \rightarrow$ Bipco $gates_1$

    $CFF_2 \rightarrow$ Bipco $gates_2$

    " " " "

    $CFF_N \rightarrow$ Bipco $gates_N$

30. Bipco-bank current driver pulse = Bipco output pulses:

    $9_{1's} + 9_{10's} + 9_{100's} + 9_{k's}$

31. $\overline{SZ\ OR} \rightarrow SFF$

D to A Conversion

The generation of the 4000 step, linear staircase is accomplished by one of the most basic D-A conversion techniques. This technique involves clocking a chain of binaries, the outputs of which are each connected to a common point through weighted resistors. The weight of each resistor is a function of the weight of each binary in the chain. The current through each resistor is summed at the common-connection point and the sum current is required to flow through an output resistor, the voltage thus generated being a staircase waveform. The precision of the staircase waveform is a function of the accuracy of the levels of the individual binaries, the accuracy of the weighting resistors, and of any reference voltage associated with the conversion process.

In this instrument, the staircase-generating binaries are arranged in four groups. The binaries of the least-significant group and the two next significant groups are connected in the BCD configuration. These BCD groups are termed UP 1's, UP 10's, and UP 100's respectively. Interconnecting these three groups in a chain provides decimal counting to 1000. The binaries of the most significant group contain two series-connected binaries providing counting to 4, the group being designated UP K's. The serial connection of all binary groups, therefore, provides counting of 4000 input pulses.

The actual conversion of the binary-stage outputs to the staircase waveform is accomplished through the use of four commercial D-A converter cards labeled LP-30. The LP-30 cards are

designed to accept BCD inputs to give a staircase output. The LP-30 card associated with the most-significant bit (MSB) group of binaries has been modified to accept only the 2^0 and 2^1 binary outputs. The modified LP-30 card must not be interchanged with any other LP-30.

A precision reference voltage of -10 volts is required for referencing the LP-30 cards. This precision reference voltage is generated through logic and will be discussed later.

One other unit is required here to complete the staircase waveform generation. This is the commercial operational amplifier named OA-30. This amplifier converts the staircase output of the LP-30's to a low-impedance, high-current output needed to drive one input of each of the 44 comparator cards. Its output capability is ± 10 volts at 20 ma. Maximum load permissible is 500 ohms and 500 pf to ground.

See the block diagram for interconnections between UP counters, LP-30's, -10 volt reference amplifier, OA-30, and comparators.

The final generated staircase-waveform is positive going, 10 volts p-p amplitude. Each staircase step is 2.5 mVpp high, the leading edge of which is coincident with a clock pulse transition.

The clock frequency is approx. 25 kc making each step width 40 us., which requires about 160 ms. for generating the complete staircase. In addition to the staircase period are the readout periods making a maximum cycle time of about 200 ms. or 5 conversion and comparison cycles per second.

Sequence of Events I

We shall start considering the sequence of events at an arbitrary step in the staircase waveform and follow through a complete cycle. Reference should be made to the timing chart. Assume that a normal cycle has been in progress and we are starting our study at a staircase step between numbers 1 and 2000.

The top waveform shows 3 staircase steps occurring before a readout cycle is initiated. In the center of each staircase step is a strobe pulse of about 5 to 10 mVpp amplitude and 1 to 5 us width sitting on top of the staircase step. This staircase waveform (positive going) is fed to one input of each differential comparator from the operational amplifier OA-30. Each unknown voltage is fed to the remaining input of each of the 44 comparators and when the differential voltage between a step on the positive staircase and an arbitrary negative unknown input-voltage is slightly more positive than zero volts, the comparator flips producing a positive voltage transition at its output. This positive-going comparator output-transition forces a latch circuit into conduction (called comparator-latch-circuit or CLC) which completely immobilizes the differential comparator for the remainder of the cycle. Refer to comparator card schematic. The triggering-into-conduction of the CLC produces a negative-going transition at its output, setting a flip-flop called comparator flip-flop or CFF.

Each comparator follows the above sequence in turn starting with the comparator whose unknown input-voltage is lowest in

magnitude and continuing to the comparator whose input voltage is greatest in magnitude. The triggering sequence of the comparators is random, dependent upon the unknown input-voltage magnitudes.

If the unknown-voltage inputs to all comparators were connected in parallel, all comparators, all CLC's, and all CFF's would simultaneously flip in turn, providing that each comparator had been calibrated correctly. Therefore, it is possible that more than one Nixie readout-bank will display the same value of equivalent input-voltage.

The outputs of all CFF's are connected in parallel through disconnect diodes and continue through an AND gate (pos. logic) on the strobe-logic card to eventually set the readout flip-flop (RFF) and delay flip-flop (DFF) on the clock-logic card.

The flipping of a differential comparator, and subsequently CLC, CFF, RFF, and DFF begins a readout cycle. The setting of RFF closes A Gate which prevents the transmission of clock pulses and thus further staircase steps from being developed.

The setting of DFF resets all first and second zero flip-flops (FZ_1, FZ_{10}, FZ_{100}, FZ_K, SZ_1, SZ_{10}, SZ_{100}, SZ_K); and DFF plus a half cycle of the clock (C) sets a special delay flip-flop (XFF) and the strobe flip-flop (SFF). The output of XFF sets another special delay flip-flop (YFF). The output of SFF produces a husky positive pulse which resets all the Bipco modules (Nixie-logic drivers), and also jams the count state of all BCD down-counters.

The UP-counters and Down-counters are arranged in groups, i.e., the "units" UP and Down counters are associated on one card, the "tens" UP and Down counters are associated on another card, etc., etc. Thus, upon completion of the JAM operation, the count state of the UP and Down counter for "units" is the same, the count state of the UP and Down counters for "tens" is the same, etc. It is realized that the groups of UP-Down counters, i.e., "units", "tens", etc. do not necessarily contain the same count, as the number stored in each counter is continuously changing from staircase level-to-level. Also, the number stored in each UP counter previous to JAMming is the BCD equivalent of the 1's, 10's, 100's, and K's of the number of steps in the staircase waveform.

Returning to XFF sets YFF, the next negative transition of the anti-clock waveform ($\overline{C}$) resets YFF whose output resets DFF. The combination RFF.$\overline{DFF}$ opens B gate allowing clock pulses to be fed through the previously opened C, D, E, and F gates.

B gate now being opened transmits clock pulse through gates C, D, E, F, to the inputs of Down counters for 1's, 10's, 100's, K's and to the inputs of the previously reset Nixie logic (Bipcos) for displaying the appropriate 1's, 10's, 100's, and K's.

B gate pulses cause each Down counter (which are backwards-counting BCD counters) to start counting backwards from the count state previously JAMmed in during the JAMming operation. As any Down counter changes count-state from count one to count zero, an output pulse is produced which flips the previously reset first-zero flip-flop (FZ_1, FZ_{10}, FZ_{100}, and/or FZ_K). The backwards

counting continues, i.e., 9, 8, 7, 6, etc. until a second one-to-zero transition occurs. Upon detection of this second "zero" FZ_N flips again, whose output flips (sets) the second-zero flip-flop (SZ_1, SZ_{10}, SZ_{100}, SZ_K). The setting of SZ_N thus indicates that two "zeros" have been counted in the backwards (down) counting scheme.

Next the setting of SZ_N plus a clock pulse sets a corresponding second-zero-delay flip-flop (SZD_1, SZD_{10}, SZD_{100}, and SZD_K) whose output closes gates C, D, E, and/or F. The sequence in which these gates close depends upon the count state of the down counters at the time of detecting the second zero. For example, if each down counter had state "2" (equalling number 2222) JAMmed in, gates C, D, E, and F would close simultaneously. If number 1803, gate E (for "0") would close first, then gate C, then F, and finally D.

Closing any of the gates C, D, E, or F, prevents clock pulses from continuing on to the Bipco units and thus discontinues Bipco counting. The last pulse entering a Bipco before closing any of these four gates decides the final count state of the Bipco unit and, therefore, the number displayed on the respective Nixie display tube.

The backward counting of the down counters provides a means of obtaining four independent serial pulse trains, the total of which have counted the number of steps generated in the staircase at the point where a readout cycle was initiated.

The completion of detecting all second zeros, plus a clock pulse, produces a group of clock pulses from the second-zero OR gate (SZ OR). The first transition produced by SZ OR resets XFF, RFF, and any CFF that was previously set.

Each bank of Bipcos has associated with it a gate controlled by a particular CFF which allows or prevents the serial pulses from gates C, D, E, or F from arriving at the Bipco input terminals. Resetting any CFF (from above) then prevents that particular Bipco unit from changing numerals the rest of the machine cycle. The next cycle, when that CFF again sets, the same Bipco bank will display the same numerals, providing that the input voltage to its associated comparator has not changed value.

The next transition of the SZ OR gate sets the strobe flip-flop (SFF). The resetting of XFF, RFF, CFF and setting SFF will allow the staircase to advance again until another readout cycle is initiated through the flipping of another comparator. The process of advancing the staircase, producing readout cycles, advancing the staircase, etc., continues until 3999 staircase steps have been produced. One more clock pulse out of the A gate will return the staircase waveform to 0000.

Sequence of Events II

The transition of the K's UP-counter from 3 to 0 (between staircase levels 3999 to 0000) flips the Pause flip-flop (PFF). PFF and the next strobe pulse sets the pause delay flip-flop (PDC). The transition occurring from the setting of the PDC initiates a special readout cycle and "forces" all comparators that have not previously flipped to flip.

This means that any comparator that had not previously been involved in a readout cycle will now be deliberately flipped and subsequently their associated CFF's. The pulse that forces these comparators to flip is called the "force" pulse and is

generated by $\overline{\text{PDC}}$. Regardless whether any comparators are forced, this special readout cycle is always initiated because $\overline{\text{PDC}}$ also sets RFF.

Following the setting of RFF, a JAM pulse is again produced (as before) JAMming the state of the UP counter into the Down counter. This time PFF is in the set state allowing the number 8000 to be JAMmed into the down counter. Thus, the forcing of any unused comparators (and CFF's) allows all unused Bipco gates to open and the number 8000 will be displayed on all Bipco modules that have not previously displayed. This cycle continues until all second zeros have again been detected and RFF, XFF, and all CFF's have been reset by $\overline{\text{SZ OR}}$.

The next half cycle of the clock generates $\overline{\text{SZ OR}}$ as before, and $\overline{\text{SZ OR}}$ resets PFF and sets SFF (as before). Resetting PFF generates a pulse called latch-reset. This pulse resets all comparator latch circuits (CLC) to the enable condition, "priming" the comparators for the start of another complete measurement cycle.

The resetting of all CLC's, then, is actually the beginning of a new DVM cycle.

The next half cycle of the clock resets PDC whose output again sets RFF, initiating another readout cycle. A strobe pulse is also generated at this time which allows any comparator to flip whose input is 0000 volts, or any comparator will flip whose input is a positive potential (wrong input polarity). All Bipco displays whose corresponding comparator input-voltage is zero or positive will now indicate 0000 because the count-state 0000 is JAMmed in

the down-counter when JAMming occurs in this part of the cycle. This cycle of events proceeds as before, detecting second zeros, closing gates C, D, E, and F, etc., and finally ending the readout cycle.

Upon completion of the above readout cycle, the staircase is again generated, a step-at-a-time until such time as an input voltage to a comparator causes it to flip, initiating a new readout cycle.

The above descriptions of the sequence of events describe the major events in a complete operation cycle of the DVM. Several other sequences of events also occur during each complete cycle which will be described below.

Staircase Reference Voltage

A precision -10 volt reference voltage is required for referencing the LP-30 D-A converter modules. This voltage is required to be stable within about 1 mv DC for many DVM operational cycles, and capable of being adjusted to -10 volts dc $\pm$ 100 mv. A precision reference was designed which would be self-calibrating and which would not require precision components. Refer to schematic #CH3954.

The philosophy of the reference amplifier is this: An operational amplifier with a very low-leakage input stage and a capacitor in the feedback loop is designed to have -10 v DC output when there is zero charge at the input terminal. The leakage rate of the input stage is low enough to allow the feedback capacitor to change its charge very slowly, therefore, changing the output voltage at a very slow rate. Two diode-pumps are

connected to the reference amplifier input terminal, one producing a positive-going voltage step under certain conditions, the other producing a negative going step under other conditions. The inputs to these diode-pump circuits are obtained from logic gates. The logic is so arranged that only one diode-pump can produce an output at a time, never simultaneously. When the logic voltages at the input of these gates indicate that the main 4000 - step staircase is too low in amplitude, one diode pump produces an output which causes the capacitor in the feedback loop to increase its charge towards -10 v (which is the LP-30 D-A converter reference voltage), generating a higher-amplitude main staircase during the next DVM operational cycle. If the logic to the diode-pump gates again indicate that the main staircase is still too low in amplitude, that diode-pump again produces an output which further increases the charge on the feedback capacitor towards -10 v. This process continues until logic indicates that no increase in reference voltage is necessary, at which time there is no input to one of the diode-pumps.

If the 4000-step staircase is too high in amplitude, logic produces an input to the other diode pump causing the feedback capacitor to be reduced in charge, a step-at-a-time until logic indicates to no further decrease in reference voltage is necessary.

The position on the staircase waveform used as a reference for the logic is step number 2000. This is obtained from one of the UP-count flip-flops in UP-Down counter #4 and is used as one of the logic inputs to the diode-pump gates.

A D.C. voltage of -5.000 volts is obtained from a temperature compensated zero diode (see schematic #CH3965). that is the input to one particular comparator (comparator #1). When this comparator is correctly calibrated and with the -5.000 volt input and a correct-amplitude main staircase input, at staircase step #2000 the comparator will flip and consequently its CFF. The CFF output from this particular comparator is another one of the inputs to the diode-pump gates.

Another input to the diode-pump gates is the output of a flip-flop called the Z flip-flop located on the -10 v reference amplifier card. It is set at staircase step #2000 and reset on the next clock pulse (at step #2001).

The diode-pump gates generate the function $\overline{K4}$. CFF . $\overline{Z}$ = pump. K4 is the #2000 staircase step transition of its UP-count flip-flop, and CFF the output of the special comparator flip-flop used for -10 v reference-voltage generation. Figure #2 shows the time relations of these various waveforms.

The input leakage current to the reference amplifier is determined from $I = \frac{C.E.}{T}$

where C = 1 uf

E = 1 mv

T = 60 sec.

$I \approx 16.7$ pA from above calculation. A very low-leakage F.E.T. was selected for the amplifier input whose max I_{gs} = 50pA. Tests on our unit indicate leakages of considerably less than this as determined from the drift rate of the reference amplifier.

Ten Pulse Detection

Another special feature of the DVM is an internal Bipco checking scheme. This scheme provides a means of continuously monitoring all Bipco counting and comparing the actual remote Bipco counting with the logic in the instrument. If a discrepancy is found between the instrument logic counting and the Bipco counting, a "tilt" lamp becomes lit indicating the miscount of some Bipco unit.

Since all the Bipcos in a particular module are reset to the same number simultaneously whenever reset occurs, and the count-pulse inputs to those Bipcos occur in parallel, Bipco counting occurs in parallel. Also, since the total number of serial pulses on any Bipco input line is the desired number plus 10 (because of detecting the first and second zeros described previously), all Bipco counting in that module passes through the number 9 (or any other numeral) simultaneously, if counting in that module is proceeding correctly.

Bipco modules produce a pulse output for each count state that the counting is passing through. See the Bipco spec sheet enclosed. In this Bipco fault detector, the number 9 output pulse from each Bipco in the display module is put into an AND gate (negative logic). See schematic #CH3963-(Ten Pulse Detector). The output of the AND gate is converted to a current pulse which is returned to the DVM rack via a coax cable. This current pulse is the converted back into a voltage pulse for use in the ten-pulse detector circuitry.

An internally generated pulse that occurs at the same time the Bipcos #9 output pulse occurs is derived from a BCD counter (called TPC). The input to this counter is down count pulses (DCP) from the logic B gate. At the count of 10, an output of the BCD counter sets a flip-flop, the output of which closes a gate at the input of TPC, preventing any more DCP's to be counted by TPC.

The 10 output of TPC, any CFF output, and the converted voltage pulse from the 9's Bipco outputs are all used as inputs to an AND gate. This gate is arranged such that no output is produced when Bipco 9's, CFF, and the 10 output of TPC occur simultaneously. If any of these gate inputs do not occur simultaneously, the gate produces an output pulse which sets a special flip-flop which has to be manually reset. The output of this flip-flop eventually drives an indicator lamp which indicates fault.

The output of the 3-input AND gate is the function

$$\text{AND } 9 \cdot \overline{\text{TPC}} \cdot \overline{\text{CFF}} = \text{tilt}$$

The timing relations of the ten pulse detector are shown in Figure #3.

LP-30 D-A Converters

Three of the commercial LP-30 D-A converter cards are used as obtained from the manufacturer. These three cards are the ones associated with the least-significant-bit up counter and the next two most-significant-bit counters (1's, 10's, 100's). The LP-30 associated with the K's up counter (most-significant-bit) has been modified to accommodate a 4-wire 2 bit binary input instead

of the usual 4-wire BCD input from the UP counters. This modification involved re-assigning the weight of the MSB in the K's group of numbers. See Appendix for LP-30 details.

OA-30 Operational Amplifier

One commercial operational amp is used to transform the medium impedance staircase waveform generated by the LP-30's to a low impedance staircase required by one input of each comparator. The OA-30 has been modified to allow the amplification to be adjustable over a small range by means of a potentiometer installed on the amplifier card. One additional resistor has been installed to allow the amplifier gain to be approximately 2.5. See the Appendix for OA-30 details and modifications.

The strobe pulses that sit in the center of each staircase step are also added to the input of the op.amp. See block diagram.

Special Comparators

Comparator #1 is permanently reserved for measuring the internal -5.000 reference potential which when compared with staircase step #2000 will (through logic) produce the -10.000 volt reference previously described required for D-A converter operation.

Comparator #2 is reserved for measuring the voltage appearing at the input of any other comparator, by means of switches described below.

Front Panel Controls

Panel #4 contains a set of two switches labeled "Input Selector" which can select any input voltage to be measured that comes into the DVM rack. There are two special positions on the

left-hand switch labeled "T" and "J". The "T" position allows a locally generated DC voltage that appears at the output of the helipot labeled "test voltage" to be switched to the input of comparator #2, providing a variable voltage for test purposes.

Position "J" allows an external voltage patched-up through the connectors labeled "test jack" to appear as the input to comparator #2. Both test jacks are in parallel so that the external-voltage input may be measured with another instrument for calibration of the DVM.

Positions #01 and #02 on these switches are not used as comparators; 1 and 2 are used for special local functions.

Panel #6 provides a jack labeled "Op. Amp." which make available the staircase waveform at the front panel, and a jack labeled "scope trig." providing a square-wave signal output for triggering an oscilloscope. The righthand side of this panel has a push button labeled "reset" which can reset the flip-flop used to hold the "failure" lamp in the on state. This failure lamp indicates a discrepancy between any Bipco readout and the internal logic as described previously.

Panel #8 has selector switches allowing the actual Bipco drive pulses from any Bipco-gate card to be sent to the right-hand display module labeled "selected output" on panel #1.

From these selectable switches, all inputs and all outputs of the DVM can be checked locally.

On the power supply panel, the red indicator lamp indicates the +200 volt power being ON and the amber lamp indicates main (low-voltage) power supply ON.

SIMPLIFIED BLOCK DIAGRAM

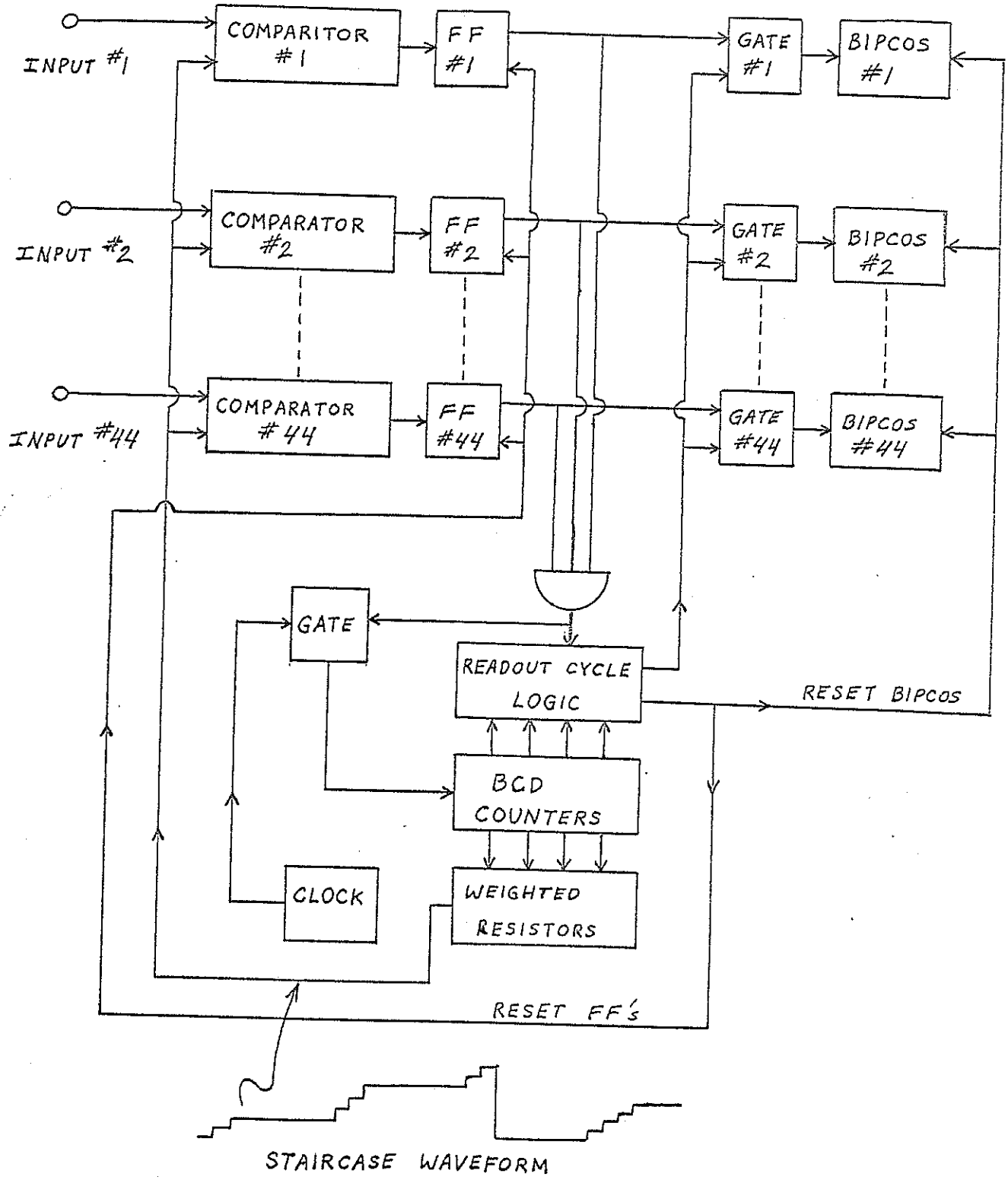

FIGURE #1

REFERENCE AMPLIFIER WAVEFORMS

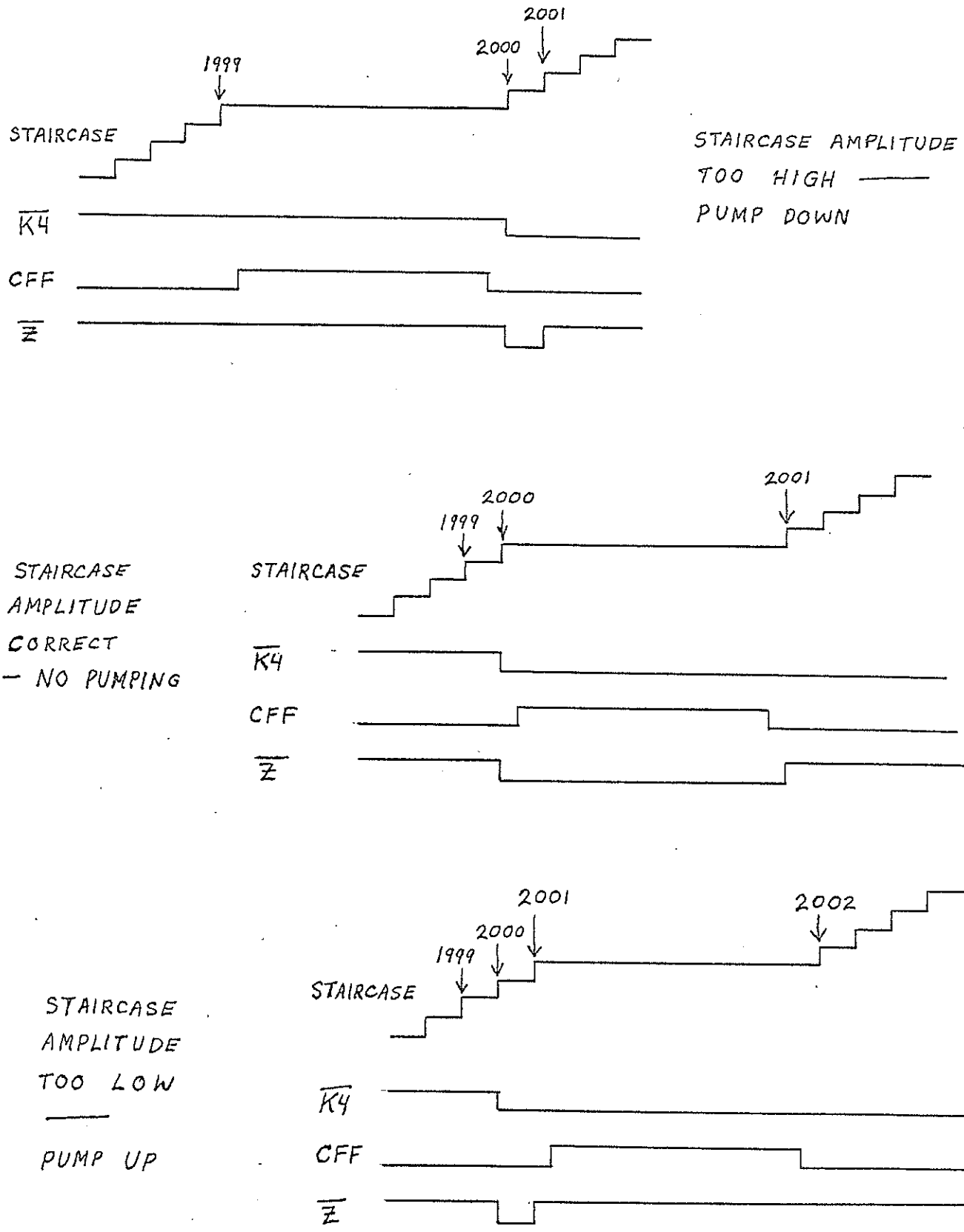

FIGURE #2.

TEN PULSE DETECTOR WAVEFORMS

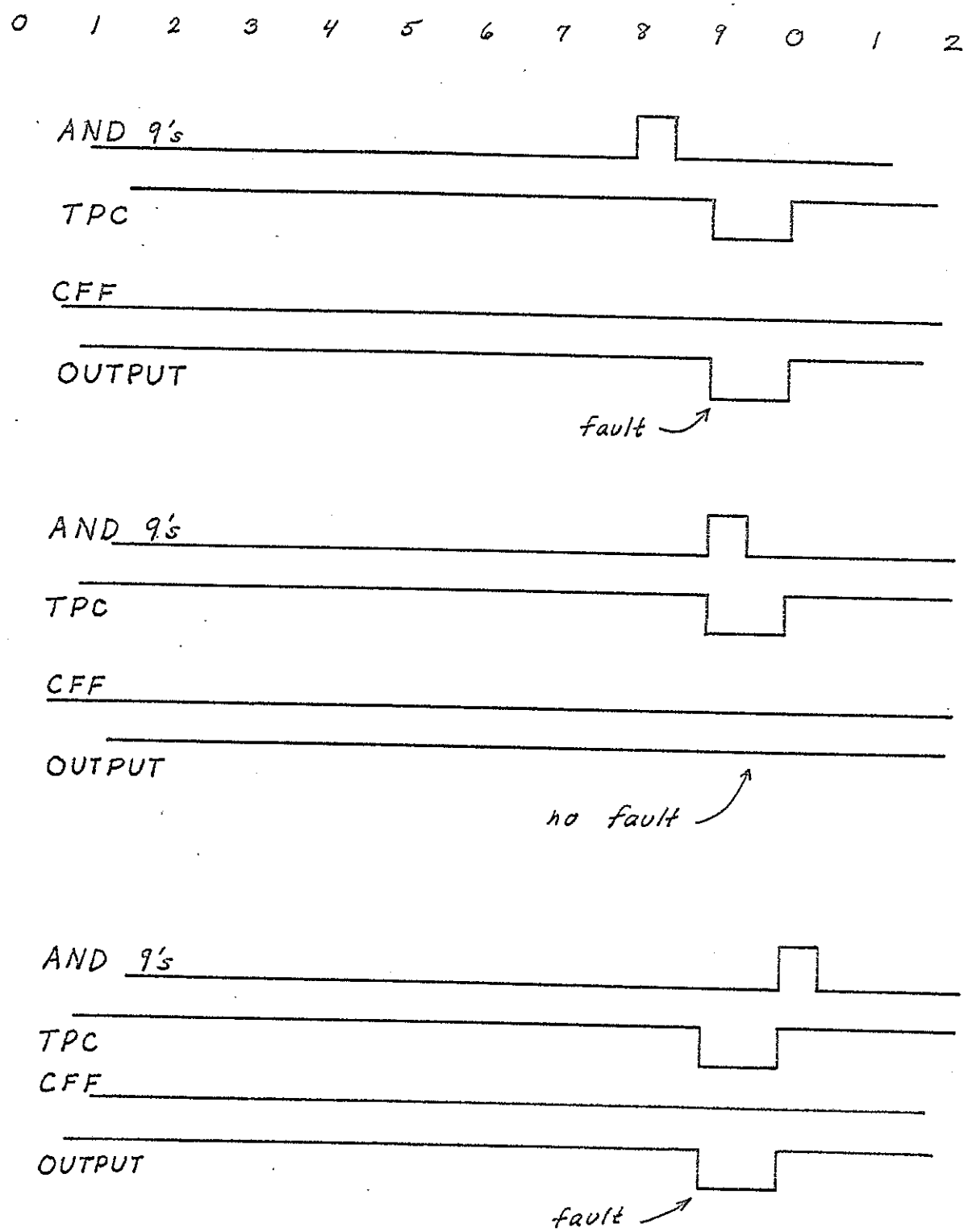

FIGURE #3