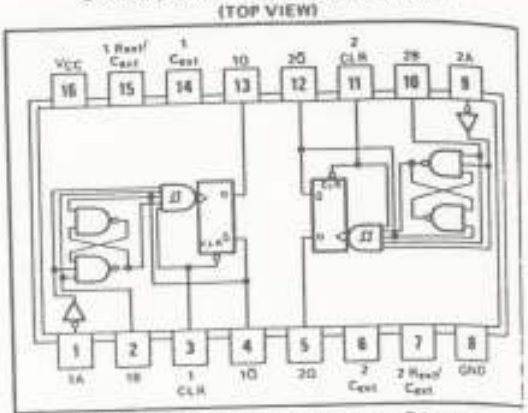
- SN54221, SN54LS221, SN74221 and SN74LS221 Are Dual Versions of Highly Stable SN54121, SN74121 One-Shots on a Monolithic Chip
- SN54221 and SN74221 Demonstrate Electrical and Switching Characteristics That Are Virtually Identical to the SN54121, SN74121 One-Shots
- Pin-Out Is Identical to the SN54123 SN74123, SN54LS123, SN74LS123
- Overriding Clear Terminates Output Pulse

SN54221, SN54LS221 . . . J OR W PACKAGE
SN74221, SN74LS221 . . . J OR N PACKAGE
(TOP VIEW)



positive logic: Low input to clear resets Q low and $\overline{Q}$ high regardless of d-c levels at A or B inputs.

TYPE	TYPICAL POWER DISSIPATION	MAXIMUM OUTPUT PULSE LENGTH
SN54221	130 mW	21 s
SN74221	130 mW	28 s
SN54LS221	23 mW	49 s
SN74LS221	23 mW	70 s

description

The '221 and 'LS221 are monolithic dual multivibrators with performance characteristics virtually identical to those of the '121. Each multivibrator features a negative-transition-triggered input and a positive-transition-triggered input either of which can be used as an inhibit input.

Pulse triggering occurs at a particular voltage level and is not directly related to the transition time of the input pulse. Schmitt-trigger input circuitry (TTL hysteresis) for B input allows jitter-free triggering from inputs with transition rates as slow as 1 volt/second, providing the circuit with excellent noise immunity of typically 1.2 volts. A high immunity to V_{CC} noise of typically 1.5 volts is also provided by internal latching circuitry.

Once fired, the outputs are independent of further transitions of the A and B inputs and are a function of the timing components, or the output pulses can be terminated by the overriding clear. Input pulses may be of any duration relative to the output pulse. Output pulse length may be varied from 35 nanoseconds to the maximums shown in the above table by choosing appropriate timing components. With R_{ext} = 2 kΩ and C_{ext} = 0, an output pulse of typically 30 nanoseconds is achieved which may be used as a d-c-triggered reset signal. Output rise and fall times are TTL compatible and independent of pulse length. Typical triggering and clearing sequences are illustrated as a part of the switching characteristics waveforms.

Pulse width stability is achieved through internal compensation and is virtually independent of V_{CC} and temperature. In most applications, pulse stability will only be limited by the accuracy of external timing components.

Jitter-free operation is maintained over the full temperature and V_{CC} ranges for more than six decades of timing capacitance (10 pF to 10 μF) and more than one decade of timing resistance (2 kΩ to 30 kΩ for the SN54221, 2 kΩ to 40 kΩ for the SN74221, 2 kΩ to 70 kΩ for the SN54LS221, and 2 kΩ to 100 kΩ for the SN74LS221). Throughout these ranges, pulse width is defined by the relationship: $t_{w(out)} = C_{ext}R_{ext}\ ln2 \approx 0.7\ C_{ext}R_{ext}$. In circuits where pulse cutoff is not critical, timing capacitance up to 1000 μF and timing resistance as low as 1.4 kΩ may be used. Also, the range of jitter-free output pulse widths is extended if V_{CC} is

FUNCTION TABLE
(EACH MONOSTABLE)

INPUTS			OUTPUTS	
CLEAR	A	B	Q	$\overline{Q}$
L	X	X	L	H
X	H	X	L	H
X	X	L	L	H
H	L	↑	⎍	⎍
H	↓	H	⎍	⎍
↑	L	H	⎍	⎍

Also see description and switching characteristics

See explanation of function tables on page 3-7

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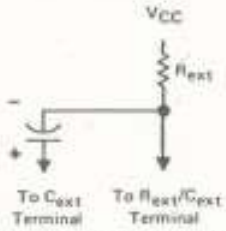
cription (continued)

...5 volts and free-air temperature is 25°C. Duty cycles as high as 90% are achieved when using maximum ...ended R_T. Higher duty cycles are available if a certain amount of pulse-width jitter is allowed.

...ariance in output pulse width from device to device is typically less than ±0.5% for given external timing ...ponents. An example of this distribution for the '221 is shown in Figure 2. Variations in output pulse width versus ...ply voltage and temperature for the '221 are shown in Figure 3 and 4, respectively.

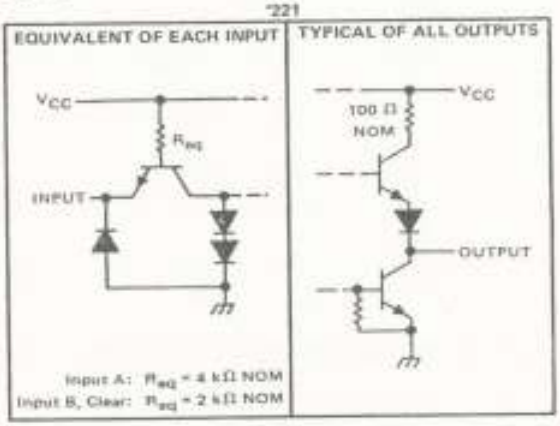
...ssignments for these devices are identical to those of the SN54123/SN74123 or SN54LS123/SN74LS123 so that ...'221 or 'LS221 can be substituted for those products in systems not using the retrigger by merely changing the ...ues of R_{ext} and/or C_{ext}.



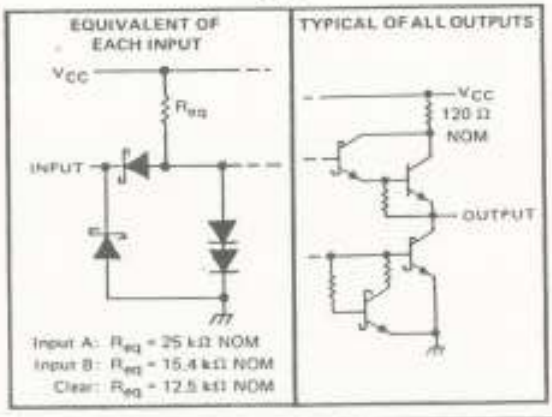
TIMING COMPONENT CONNECTIONS

...matics of inputs and outputs

'221



'LS221



recommended operating conditions

		SN54221			SN74221			UNIT
		MIN	NOM	MAX	MIN	NOM	MAX	
Supply voltage, V_{CC}		4.5	5	5.5	4.75	5	5.25	V
High-level output current, I_{OH}				−800			−800	μA
Low-level output current, I_{OL}				16			16	mA
Rate of rise or fall of input pulse, dv/dt	Schmitt input, B	1			1			V/s
	Logic input, A	1			1			V/μs
Input pulse width	A or B, $t_{w(in)}$	50			50			ns
	Clear, $t_{w(clear)}$	20			20			
Clear-inactive-state setup time, t_{su}		15			15			ns
External timing resistance, R_{ext}		1.4		30	1.4		40	kΩ
External timing capacitance, C_{ext}		0		1000	0		1000	pF
Output duty cycle	R_{ext} = 2 kΩ			67			67	%
	R_{ext} = MAX R_{ext}			90			90	
Operating free-air temperature, T_A		−55		125	0		70	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS†		MIN	TYP‡	MAX	UNIT
V_{T+}	Positive-going threshold voltage at A input	V_{CC} = MIN			1.4	2	V
V_{T-}	Negative-going threshold voltage at A input	V_{CC} = MIN		0.8	1.4		V
V_{T+}	Positive-going threshold voltage at B input	V_{CC} = MIN			1.55	2	V
V_{T-}	Negative-going threshold voltage at B input	V_{CC} = MIN		0.8	1.35		V
V_{IK}	Input clamp voltage	V_{CC} = MIN, I_I = −12 mA				−1.5	V
V_{OH}	High-level output voltage	V_{CC} = MIN, I_{OH} = −800 μA		2.4	3.4		V
V_{OL}	Low-level output voltage	V_{CC} = MIN, I_{OL} = 16 mA			0.2	0.4	V
I_I	Input current at maximum input voltage	V_{CC} = MAX, V_I = 5.5 V				1	mA
I_{IH}	High-level input current	V_{CC} = MAX, V_I = 2.4 V	Input A			40	μA
			Input B, Clear			80	
I_{IL}	Low-level input current	V_{CC} = MAX, V_I = 0.4 V	Input A			−1.6	mA
			Input B, Clear			−3.2	
I_{OS}	Short-circuit output current§	V_{CC} = MAX	SN54221	−20		−55	mA
			SN74221	−18		−55	
I_{CC}	Supply current	V_{CC} = MAX	Quiescent		26	50	mA
			Triggered		46	80	

†For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.
‡All typical values are at V_{CC} = 5 V, T_A = 25°C.
§Not more than one output should be shorted at a time.

switching characteristics, V_{CC} = 5 V, T_A = 25°C

PARAMETER¶	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS		MIN	TYP	MAX	UNIT
t_{PLH}	A	Q	C_L = 15 pF, R_L = 400 Ω, See Figure 1 and Note 2	C_{ext} = 80 pF, R_{ext} = 2 kΩ		45	70	ns
	B	Q				35	55	
t_{PHL}	A	$\overline{Q}$				60	80	ns
	B	$\overline{Q}$				40	65	
t_{PHL}	Clear	Q				27		ns
t_{PLH}	Clear	$\overline{Q}$				40		ns
$t_{w(out)}$	A or B	Q or $\overline{Q}$		C_{ext} = 80 pF, R_{ext} = 2 kΩ	70	110	150	ns
				C_{ext} = 0, R_{ext} = 2 kΩ	20	30	50	
				C_{ext} = 100 pF, R_{ext} = 10 kΩ	650	700	750	
				C_{ext} = 1 μF, R_{ext} = 10 kΩ	6.5	7	7.5	ms

¶t_{PLH} = Propagation delay time, low-to-high-level output
t_{PHL} = Propagation delay time, high-to-low-level output
$t_{w(out)}$ = Output pulse width
NOTE 2: Load circuit is shown on page 3-10.

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switching characteristics, V_{CC} = 5 V, T_A = 25°C

PARAMETER¶	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS		MIN	TYP	MAX	UNIT
t_{PLH}	A	Q	C_L = 15 pF, R_L = 2 kΩ, See Figure 1 and Note 3	C_{ext} = 80 pF, R_{ext} = 2 kΩ		45	70	ns
	B	Q				35	55	
t_{PHL}	A	$\overline{Q}$				50	80	ns
	B	$\overline{Q}$				40	65	
t_{PHL}	Clear	Q				35	55	ns
t_{PLH}	Clear	$\overline{Q}$				44	65	ns
$t_{w(out)}$	A or B	Q or $\overline{Q}$		C_{ext} = 80 pF, R_{ext} = 2 kΩ	70	120	150	ns
				C_{ext} = 0, R_{ext} = 2 kΩ	20	47	70	
				C_{ext} = 100 pF, R_{ext} = 10 kΩ	600	670	750	
				C_{ext} = 1 μF, R_{ext} = 10 kΩ	6	6.9	7.5	ms

¶ t_{PLH} = Propagation delay time, low-to-high-level output
t_{PHL} = Propagation delay time, high-to-low-level output
$t_{w(out)}$ = Output pulse width

NOTE 3: Load circuit is shown on page 3-11.

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recommended operating conditions

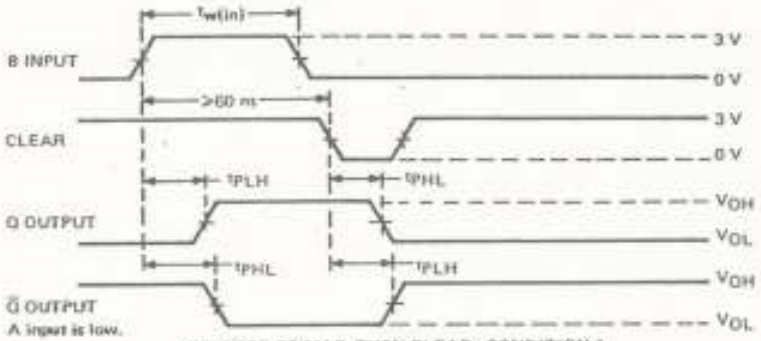
			SN54LS221			SN74LS221			UNIT
			MIN	NOM	MAX	MIN	NOM	MAX	
Supply voltage, V_{CC}			4.5	5	5.5	4.75	5	5.25	V
High-level output current, I_{OH}					−400			−400	μA
Low-level output current, I_{OL}					4			8	mA
Rate of rise or fall of input pulse, dv/dt		Schmitt, B	1			1			V/s
		Logic input, A	1			1			V/μs
Input pulse width		A or B, $t_{w(in)}$	40			40			ns
		Clear, $t_{w(clear)}$	40			40			
Clear-inactive-state setup time, t_{su}			15			15			ns
External timing resistance, R_{ext}			1.4		70	1.4		100	kΩ
External timing capacitance, C_{ext}			0		1000	0		1000	μF
Output duty cycle		R_T = 2 kΩ			50			50	%
		R_T = MAX R_{ext}			90			90	
Operating free-air temperature, T_A			−55		125	0		70	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

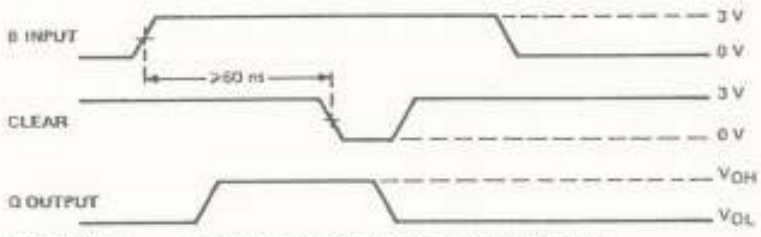
PARAMETER		TEST CONDITIONS†		SN54LS221			SN74LS221			UNIT
				MIN	TYP‡	MAX	MIN	TYP‡	MAX	
V_{T+}	Positive-going threshold voltage at A input	V_{CC} = MIN			1.0	2		1.0	2	V
V_{T-}	Negative-going threshold voltage at A input	V_{CC} = MIN		0.7	1.0		0.8	1.0		V
V_{T+}	Positive-going threshold voltage at B input	V_{CC} = MIN			1.0	2		1.0	2	V
V_{T-}	Negative-going threshold voltage at B input	V_{CC} = MIN		0.7	0.9		0.8	0.9		V
V_{IK}	Input clamp voltage	V_{CC} = MIN, I_I = −18 mA				−1.5			−1.5	V
V_{OH}	High-level output voltage	V_{CC} = MIN, I_{OH} = −400 μA		2.5	3.4		2.7	3.4		V
V_{OL}	Low-level output voltage	V_{CC} = MIN	I_{OL} = 4 mA		0.25	0.4		0.25	0.4	V
			I_{OL} = 8 mA					0.35	0.5	
I_I	Input current at maximum input voltage	V_{CC} = MAX, V_I = 7 V				0.1			0.1	mA
I_{IH}	High-level input current	V_{CC} = MAX, V_I = 2.7 V				20			20	μA
I_{IL}	Low-level input current	Input A	V_{CC} = MAX, V_I = 0.4 V			−0.4			−0.4	mA
		Input B				−0.8			−0.8	
		Clear				−0.8			−0.8	
I_{OS}	Short-circuit output current§	V_{CC} = MAX		−20		−100	−20		−100	mA
I_{CC}	Supply current	V_{CC} = MAX	Quiescent		4.7	11		4.7	11	mA
			Triggered		19	27		19	27	

†For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.
‡All typical values are at V_{CC} = 5 V, T_A = 25°C.
§Not more than one output should be shorted at a time, and duration of the short-circuit should not exceed one second.

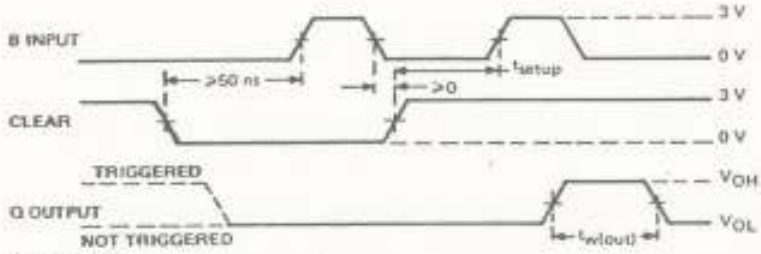
PARAMETER MEASUREMENT INFORMATION



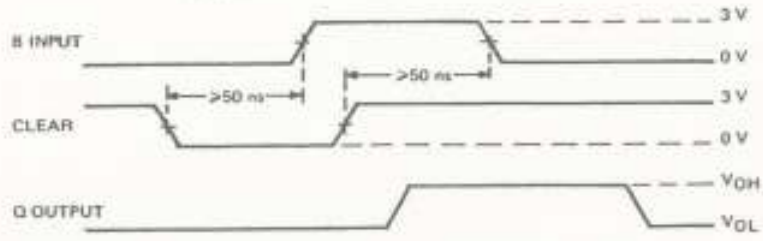
TRIGGER FROM B, THEN CLEAR–CONDITION 1



TRIGGER FROM B, THEN CLEAR–CONDITION 2



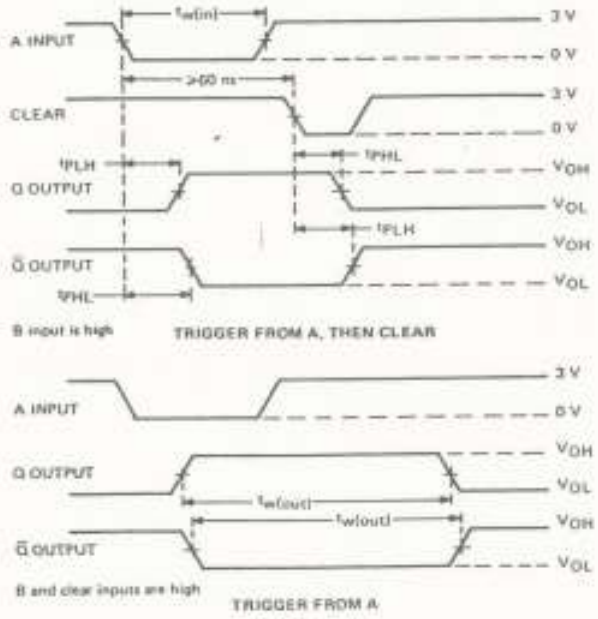
CLEAR OVERRIDING B, THEN TRIGGER FROM B



TRIGGERING FROM POSITIVE TRANSITION OF CLEAR

FIGURE 1–SWITCHING CHARACTERISTICS

PARAMETER MEASUREMENT INFORMATION



NOTES: A. Input pulses are supplied by generators having the following characteristics: PRR ≤ 1 MHz, Z_{out} = 50 Ω; for '221, t_r = t_f ≤ 7 ns, for 'LS221, t_r ≤ 15 ns, t_f ≤ 6 ns.
B. All measurements are made between the 1.5 V points of the indicated transitions for the '221 or between the 1.3 V points for the 'LS221.

FIGURE 1–SWITCHING CHARACTERISTICS (CONTINUED)

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TYPICAL CHARACTERISTICS ('221 ONLY)†

DISTRIBUTION OF UNITS
for
OUTPUT PULSE WIDTH

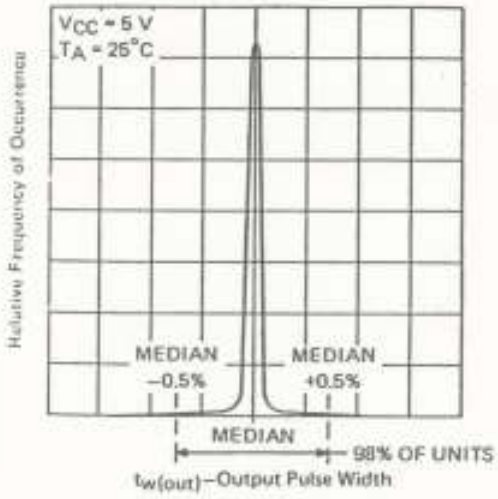

FIGURE 2

VARIATION IN OUTPUT PULSE WIDTH
vs
SUPPLY VOLTAGE

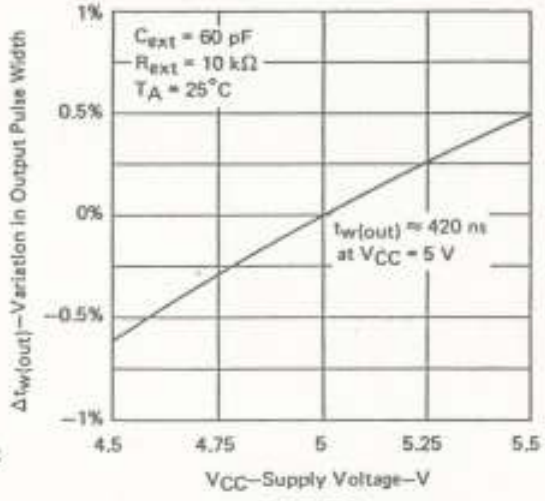

FIGURE 3

VARIATION IN OUTPUT PULSE WIDTH
vs
FREE-AIR TEMPERATURE

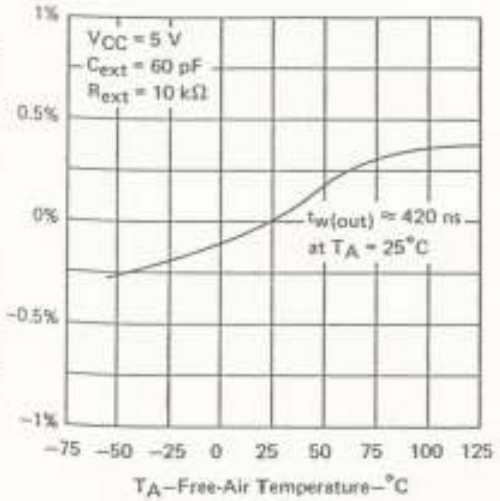

FIGURE 4

OUTPUT PULSE WIDTH
vs
TIMING RESISTOR VALUE

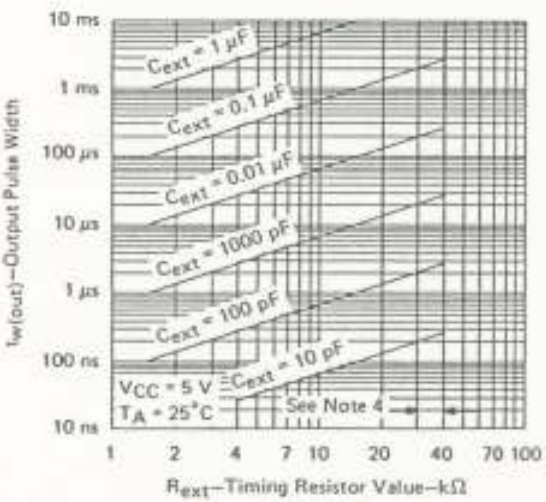

FIGURE 5

† These values of resistance exceed the maximum recommended for use over the full temperature range of the SN54221.
For temperatures below 0°C and above 70°C, and for supply voltages below 4.75 V and above 5.25 V are applicable for the SN54221