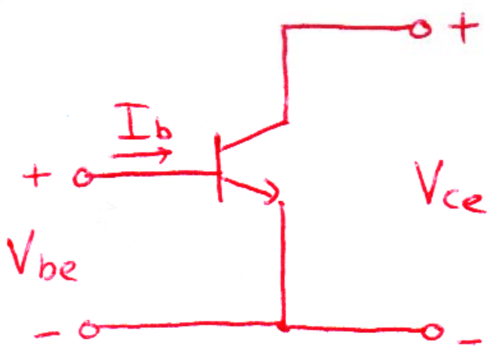
P3360/AEP3630

Lecture 16

Transistors (BJT's)

3 terminals ⇒ one terminal common to input & output

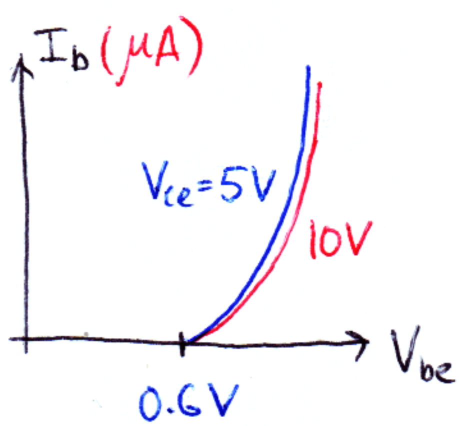
Common emitter configuration (one of 3 possibilities)



$V_{be} \equiv V_b - V_e$

$V_{ce} \equiv V_c - V_e$

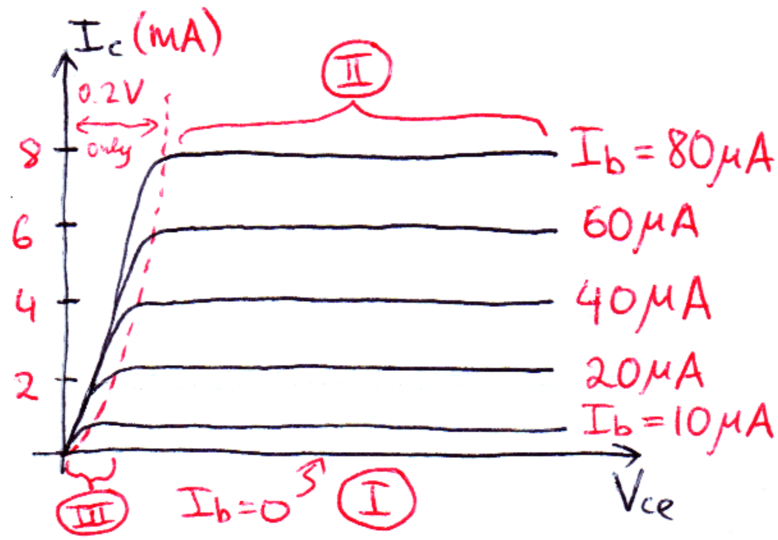
input characteristics



- like forward biased diode
- weak dependence on V_{ce}

output (3 modes)

	be-junct.	bc-junct.
I cutoff	reverse	reverse
II active	forward	reverse
III satur.	forward	forward



I cutoff (OFF) $I_b \sim 0$, $V_{be} < 0.6V$ (reverse), $I_c \sim 0$

~ open circuit between c & e

II active
normal op. mode

$I_b > 0$, $V_{be} \gtrsim 0.6V$ (forward)

$V_{bc} \ll 0.4V$ (reverse)

$I_c = \beta I_b$ ($\beta \gg 1$), I_c indep of V_{ce}

current controlled current source

III saturation (ON) $I_b > 0$, $V_{be} \gtrsim 0.6V$, $V_{bc} \gtrsim 0.4V$ (forward)

$V_{ce\text{-}sat} \sim 0.1\text{-}0.2V$ (small) ← check spec. sheets

~ short between c & e

I_c is as large as external circuit allows

Important notes:

β – unreliable parameter, varies with T, from transistor to transistor

$$\beta_{dc} = \frac{I_c}{I_b} \qquad \beta_{ac} = \frac{\Delta I_c}{\Delta I_b}$$

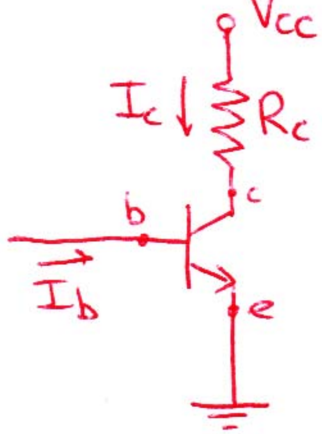
e.g. $\beta_{ac} \uparrow$ as $I_b, I_c \uparrow$ @ fixed V_{ce}

I_b			
	0.5 – 5 μA	$\beta_{ac} \to 2\beta_{ac}$	see spec. sheets
	5 – 50 μA	$\beta_{ac} \to 1.1\beta_{ac}$	

β is garanteed to be $\boxed{\beta \gg 1}$

Sometimes denoted by $\beta = h_{fe}$ ← other common notation
(f = forward, e = emitter)

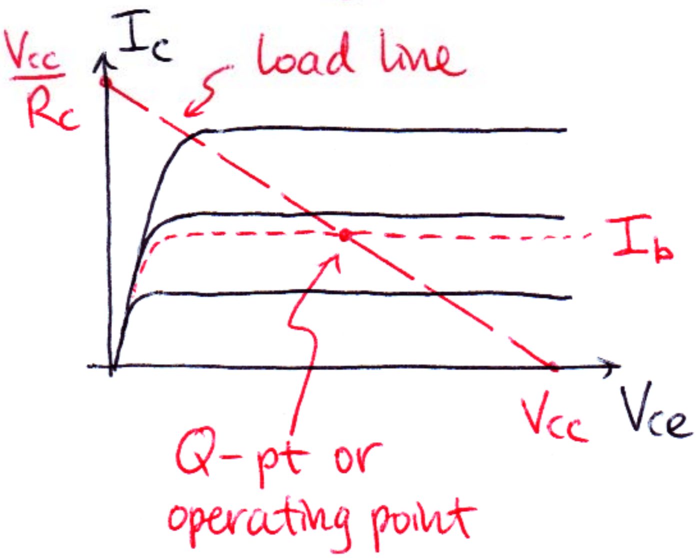
Transistor circuits



V_{cc} ← "cc" - collector p.s. voltage ("ee" - emitter p.s. volt.)

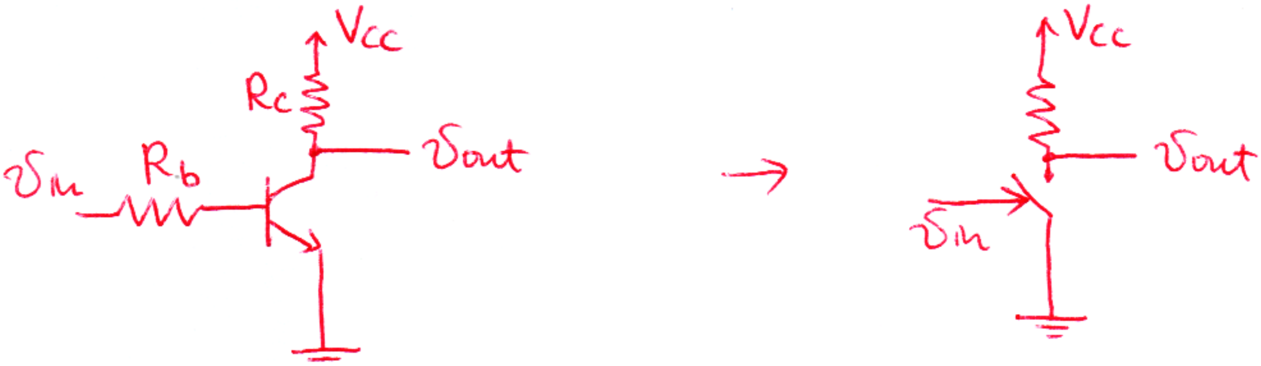
KVL: $V_{cc} - R_c I_c - V_{ce} = 0$

$$\Rightarrow \boxed{I_c = -\frac{V_{ce}}{R_c} + \frac{V_{cc}}{R_c}}$$ "load line"



- op. point (Q) constrained to lie on load line
- Q pt for V_{cc}, R_c fixed is determined by I_b

Transistor switch (a.k.a. saturating inverter)



i) $v_{in} < 0\,V$, $I_b \sim 0$, $I_c \sim 0$ $v_{out} = V_{cc}$ (HI)

switch open

ask

2) $v_{in} \gg 0.6V$ $(V_{be} \sim 0.6V)$, $\Rightarrow$ I_b is large

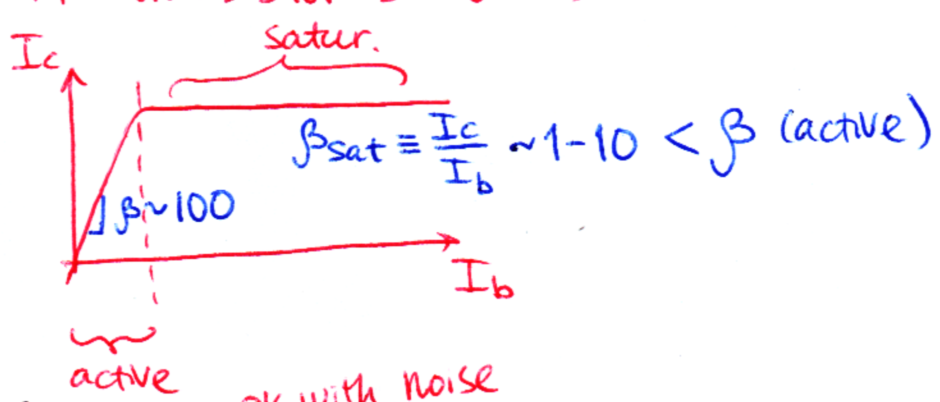
V_{ce} ? see load line & I_c vs. V_{ce} plot $\Rightarrow$ saturation

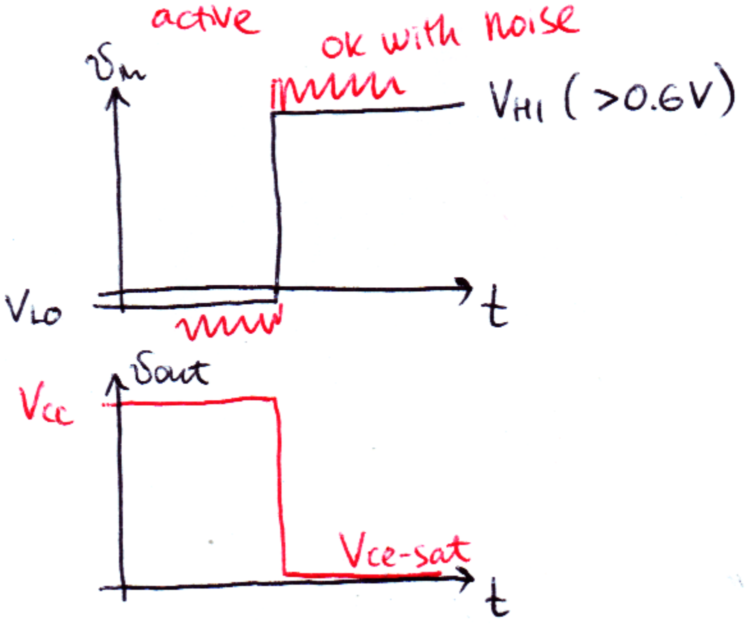
$V_{ce} \simeq V_{ce\text{-}sat}$ $(0.2V)$, $v_{out} = 0.2V$ (LO)

switch closed

Q: $I_c = \beta \cdot I_b$ when active. What if $I_c > \frac{V_{cc}}{R_c}$ (or $I_b > \frac{V_{cc}}{R_c \beta}$?)

A: transistor saturates





Important:

care must be given in choosing R_b

$\beta_{min} < \beta < \beta_{max}$ (β value uncertain)

To ensure saturation for $v_{in} = V_{HI}$

choose

$$(I_b)_{sat} \geq \frac{(I_c)_{sat}}{\beta_{min}} = \frac{V_{cc}}{R_c} \frac{1}{\beta_{min}}, \Rightarrow$$

$I_b \cdot R_b = v_{in} - 0.6V$,

$$\text{choose} \quad R_b \leq \frac{V_{HI} - 0.6V}{(I_b)_{sat}}$$