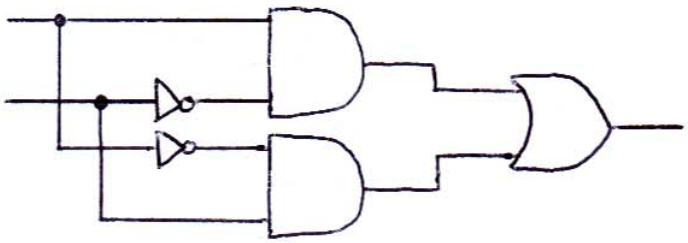
Lecture 25

XOR gate

A	B	X
0	0	
0	1	
1	0	
1	1	



Design procedure for combinational logic circuits

1) assign symbols

2) obtain boolean fcn
   a)
   b)
3) [optional]
4) draw the schematic

T	P	S	H
0	0	0	0
0	0	1	1
0	1	0	0
0	1	1	1
1	0	0	1
1	0	1	1
1	1	0	0
1	1	1	1

minterms –

maxterms –

output =

output =

Simplifying boolean expressions with Karnaugh maps ③

Consider 2-input fcn

A	B	minterm
0	0	
0	1	
1	0	
1	1	

$\bar{A}\cdot\bar{B}$	$\bar{A}\cdot B$
$A\cdot\bar{B}$	$A\cdot B$

$\bar{A}\cdot\bar{B}$	$\bar{A}\cdot B$
$A\cdot\bar{B}$	$A\cdot B$

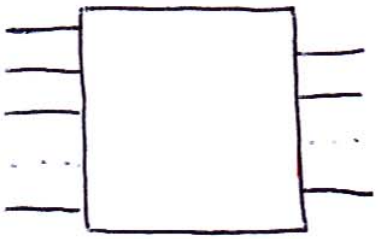
3-input fcn

4-input fcn

S \ TP	00	01	11	10
0				
1				

Programmable logic devices

- used to implement



- can generate

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- some PLD types :