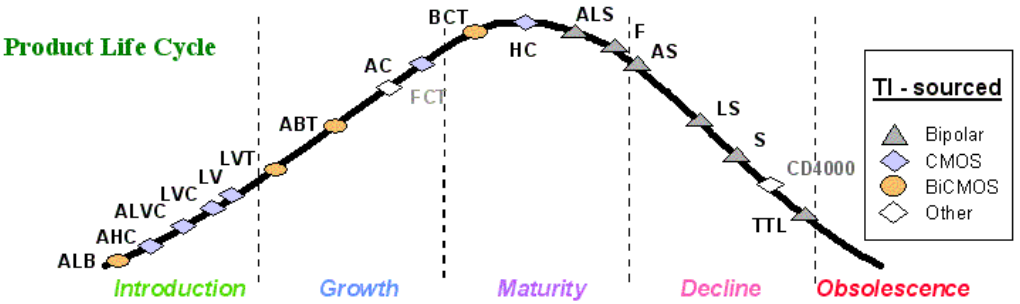


Digital Logic Families

PHYS3360/AEP3630

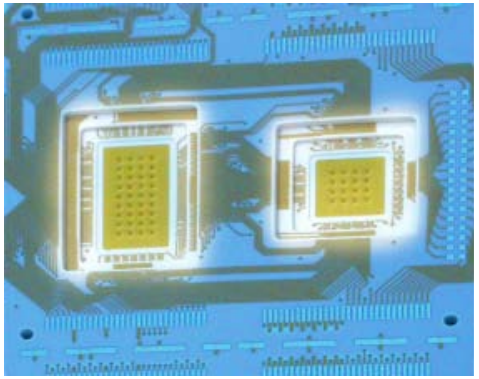
Lecture 26

Overview

- Integration, Moore’s law
- Early families (DL, RTL)
- TTL
- Evolution of TTL family
- ECL
- CMOS family and its evolution
- Overview

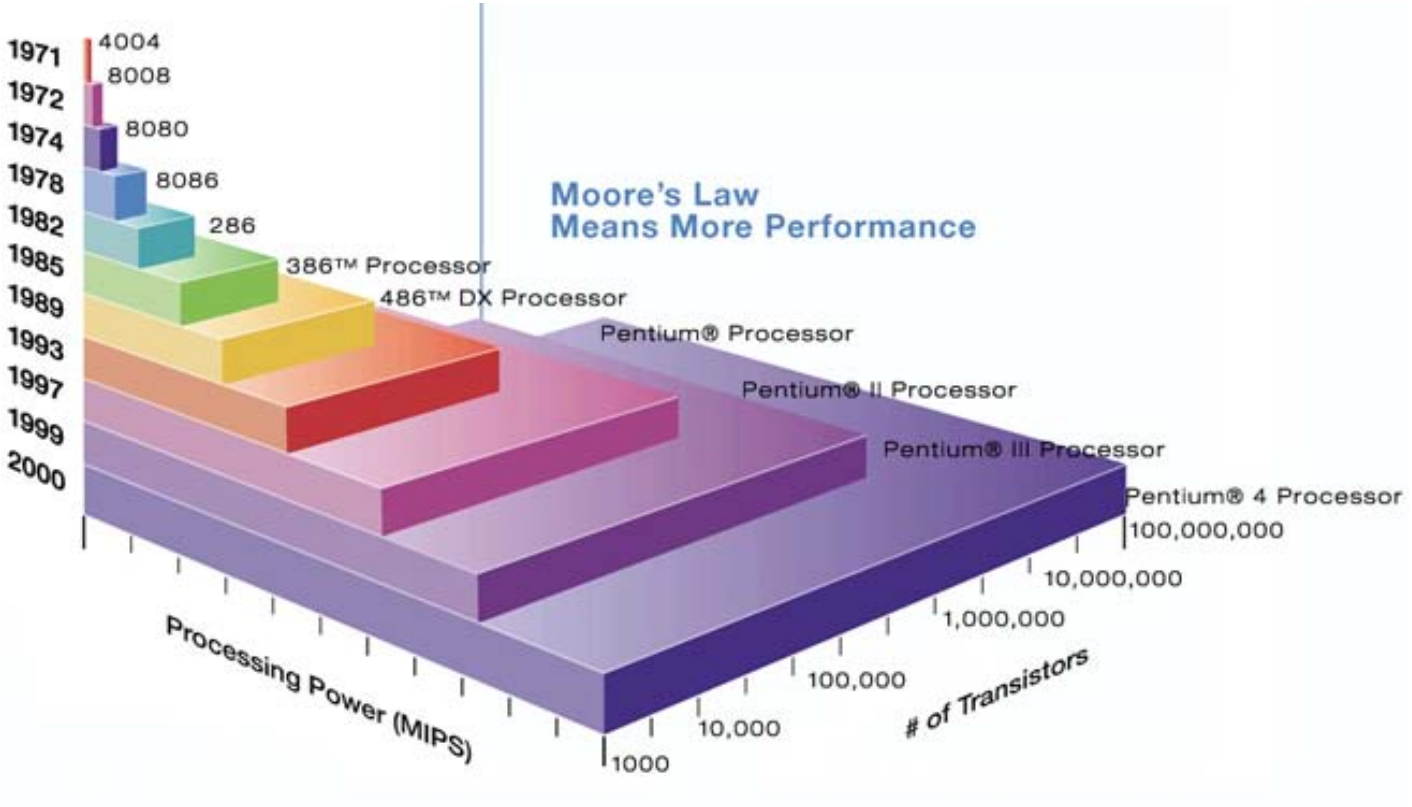
Integration Levels

- Gate/transistor ratio is roughly 1/10
  - SSI < 12 gates/chip
  - MSI < 100 gates/chip
  - LSI …1K gates/chip
  - VLSI …10K gates/chip
  - ULSI …100K gates/chip
  - GSI …1Meg gates/chip



Moore’s law

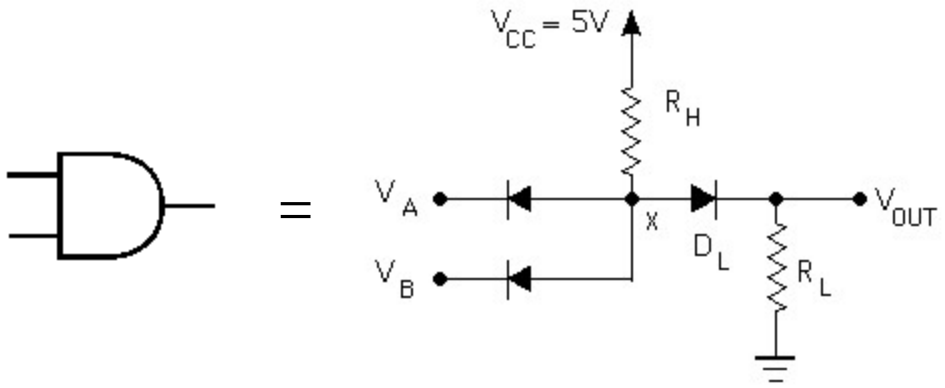
- A prediction made by Moore (a co-founder of Intel) in 1965: “… a number of transistors to double every 2 years.”



In the beginning…

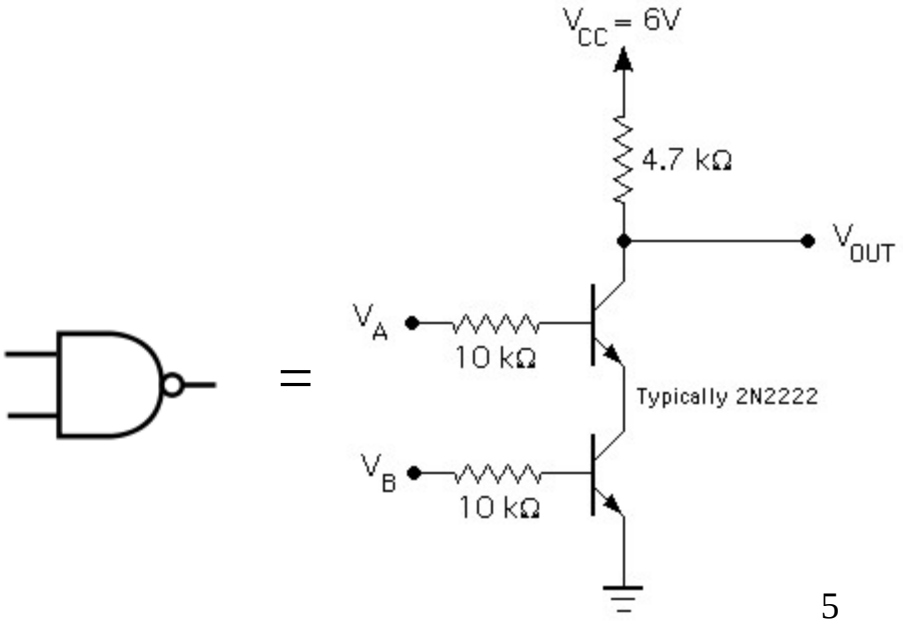
Diode Logic (DL)

- simplest; does not scale
- NOT not possible (need an active element)



Resistor-Transistor Logic (RTL)

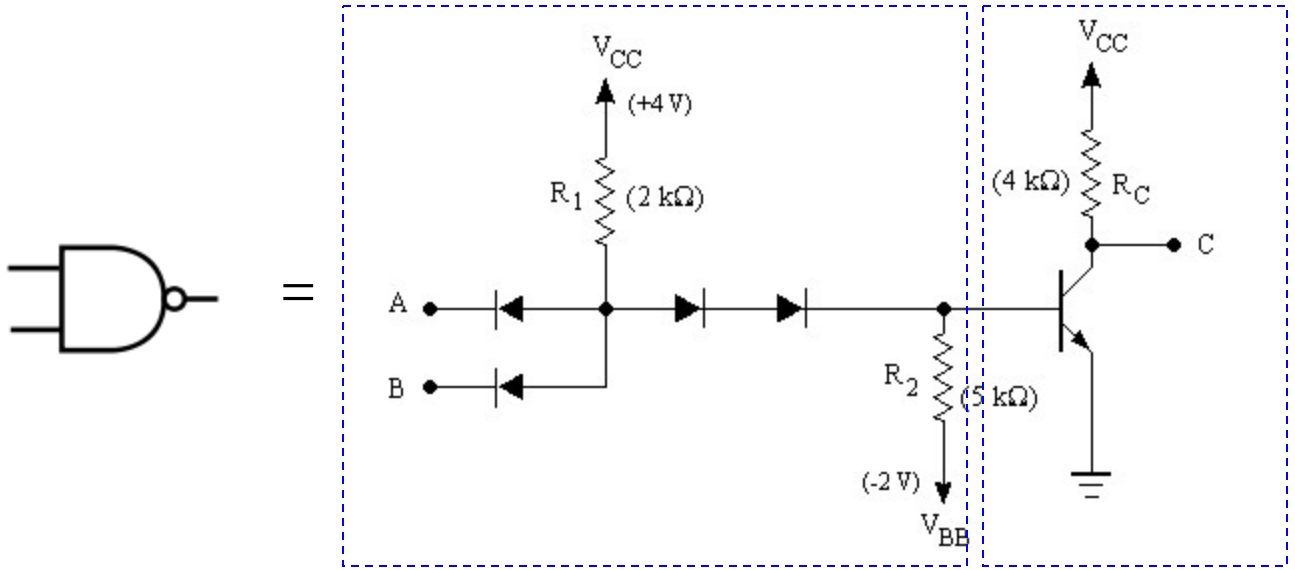
- replace diode switch with a transistor switch
- can be cascaded
- large power draw



was…

Diode-Transistor Logic (DTL)

- essentially diode logic with transistor amplification
- reduced power consumption
- faster than RTL



DL AND gate

Saturating inverter

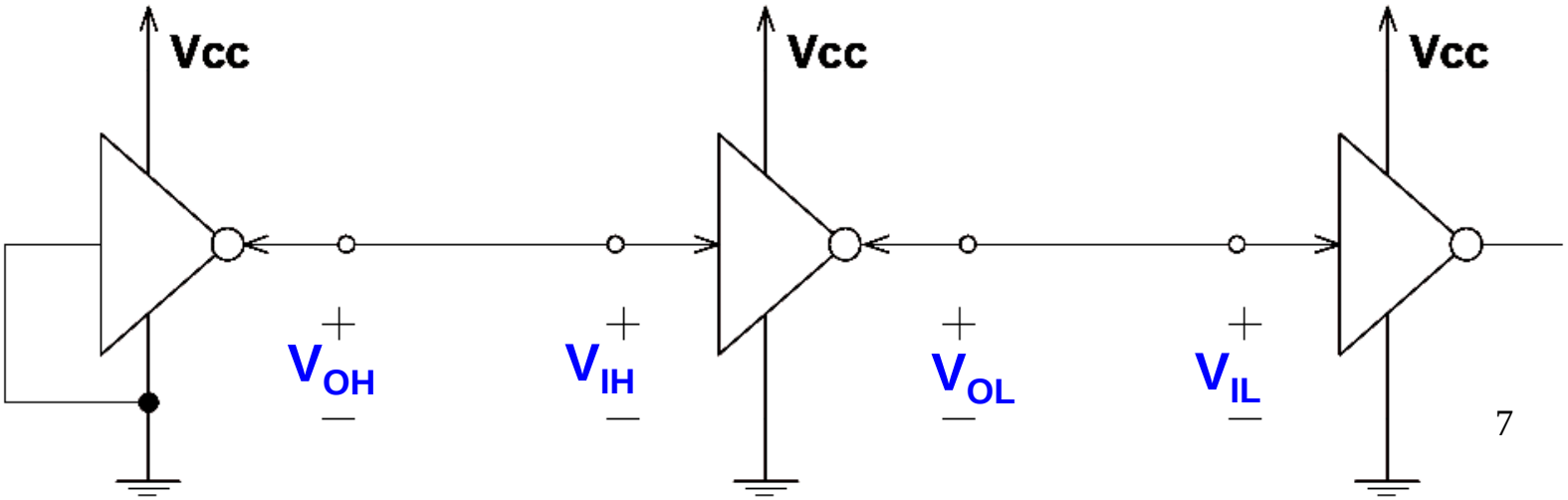
Logic families: V levels

V_{OH}(min) – The minimum voltage level at an output in the logical "1" state under defined load conditions

V_{OL}(max) – The maximum voltage level at an output in the logical "0" state under defined load conditions

V_{IH}(min) – The minimum voltage required at an input to be recognized as "1" logical state

V_{IL}(max) – The maximum voltage required at an input that still will be recognized as "0" logical state



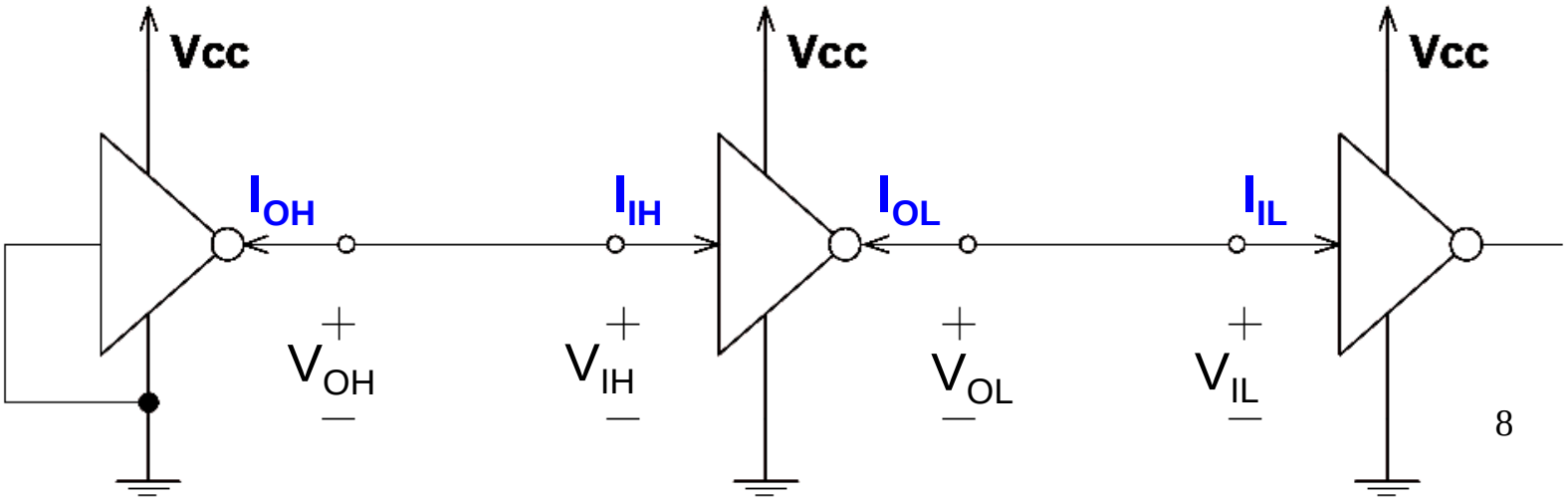
Logic families: I requirements

I_{OH} – Current flowing into an output in the logical “1” state under specified load conditions

I_{OL} – Current flowing into an output in the logical “0” state under specified load conditions

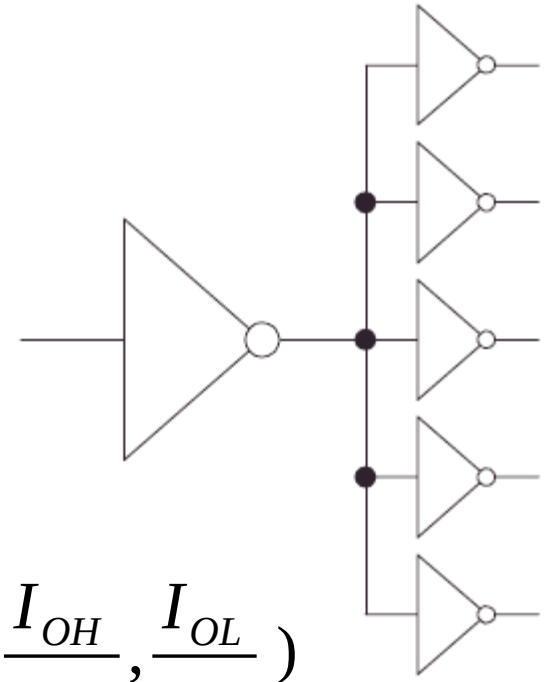
I_{IH} – Current flowing into an input when a specified HI level is applied to that input

I_{IL} – Current flowing into an input when a specified LO level is applied to that input



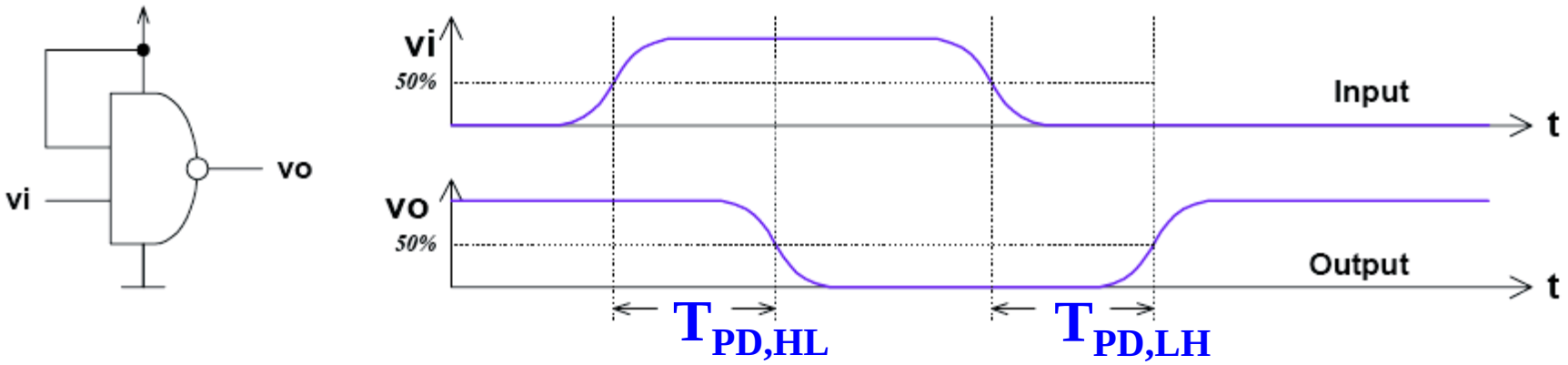
Logic families: fanout

Fanout: the maximum number of logic inputs (of the same logic family) that an output can drive reliably



DC fanout = $\min\left(\frac{I_{OH}}{I_{IH}}, \frac{I_{OL}}{I_{IL}}\right)$

Logic families: propagation delay

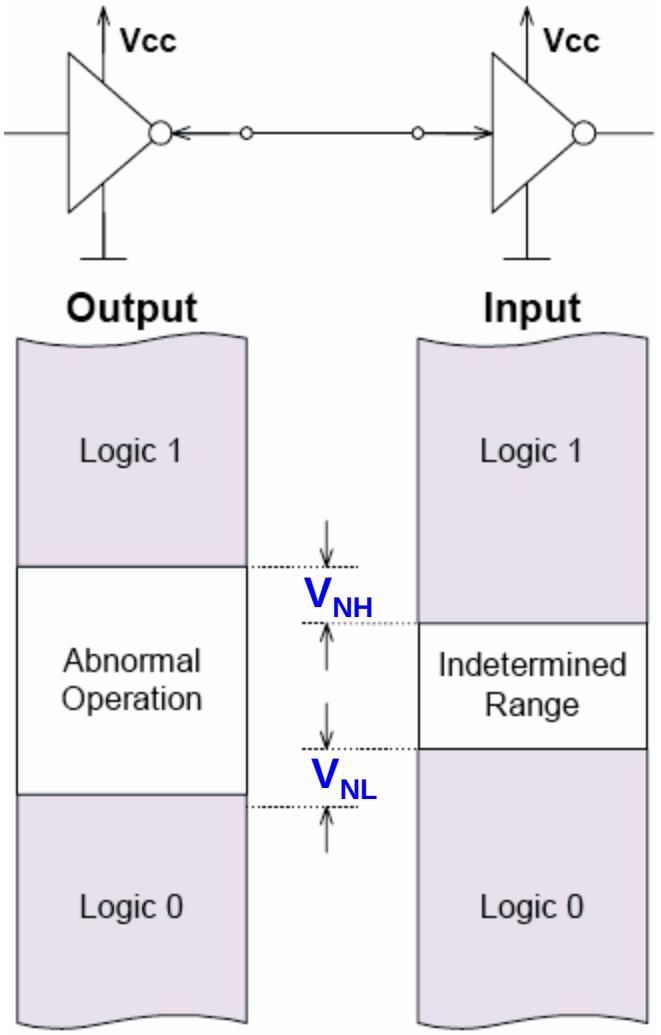


$T_{PD,HL}$ – input-to-output propagation delay from HI to LO output

$T_{PD,LH}$ – input-to-output propagation delay from LO to HI output

Speed-power product: $T_{PD} \times P_{avg}$

Logic families: noise margin



HI state noise margin:

$V_{NH} = V_{OH}(min) - V_{IH}(min)$

LO state noise margin:

$V_{NL} = V_{IL}(max) - V_{OL}(max)$

Noise margin:

$V_N = min(V_{NH}, V_{NL})$

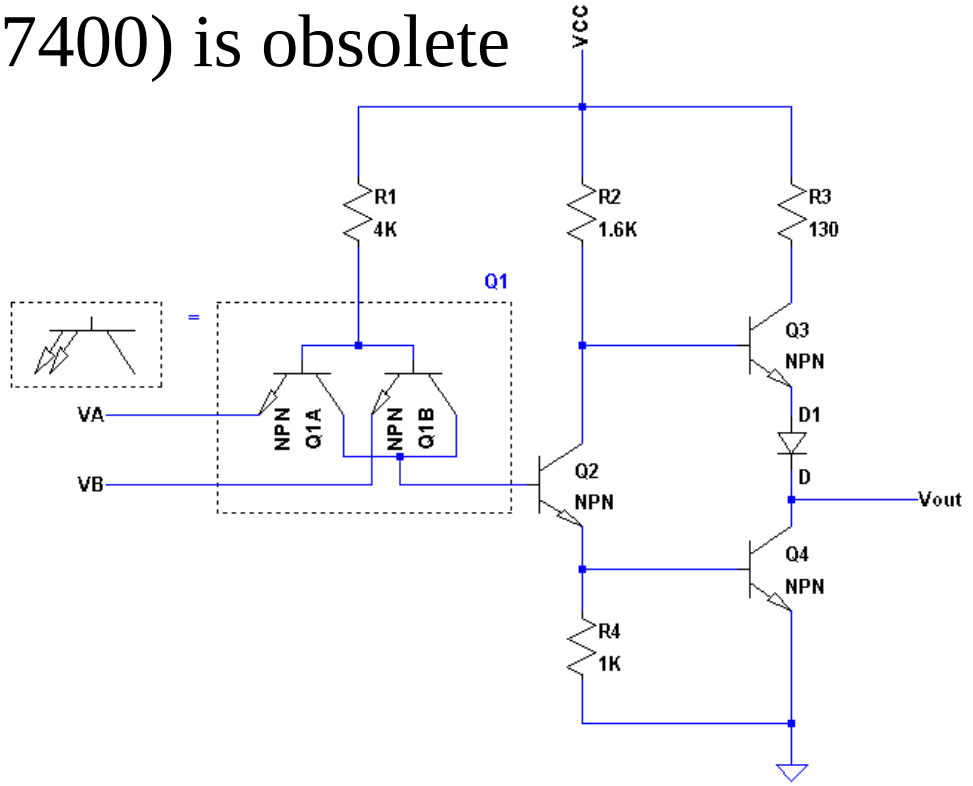
TTL

Bipolar Transistor-Transistor Logic (TTL)

- first introduced by in 1964 (Texas Instruments)
- TTL has shaped digital technology in many ways
- Standard TTL family (e.g. 7400) is obsolete
- Newer TTL families still used (e.g. 74ALS00)

Distinct features

- Multi-emitter transistors
- Totem-pole transistor arrangement
- Open LTspice example: TTL NAND…



2-input NAND

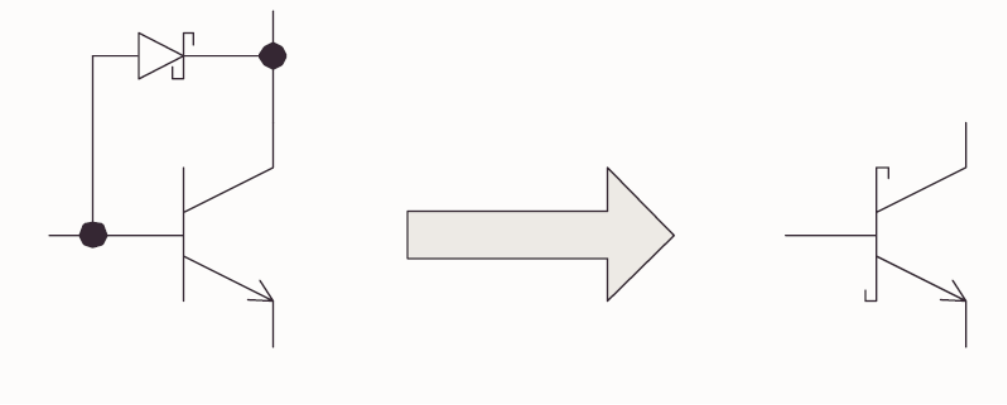
TTL evolution

Schottky series (74LS00) TTL

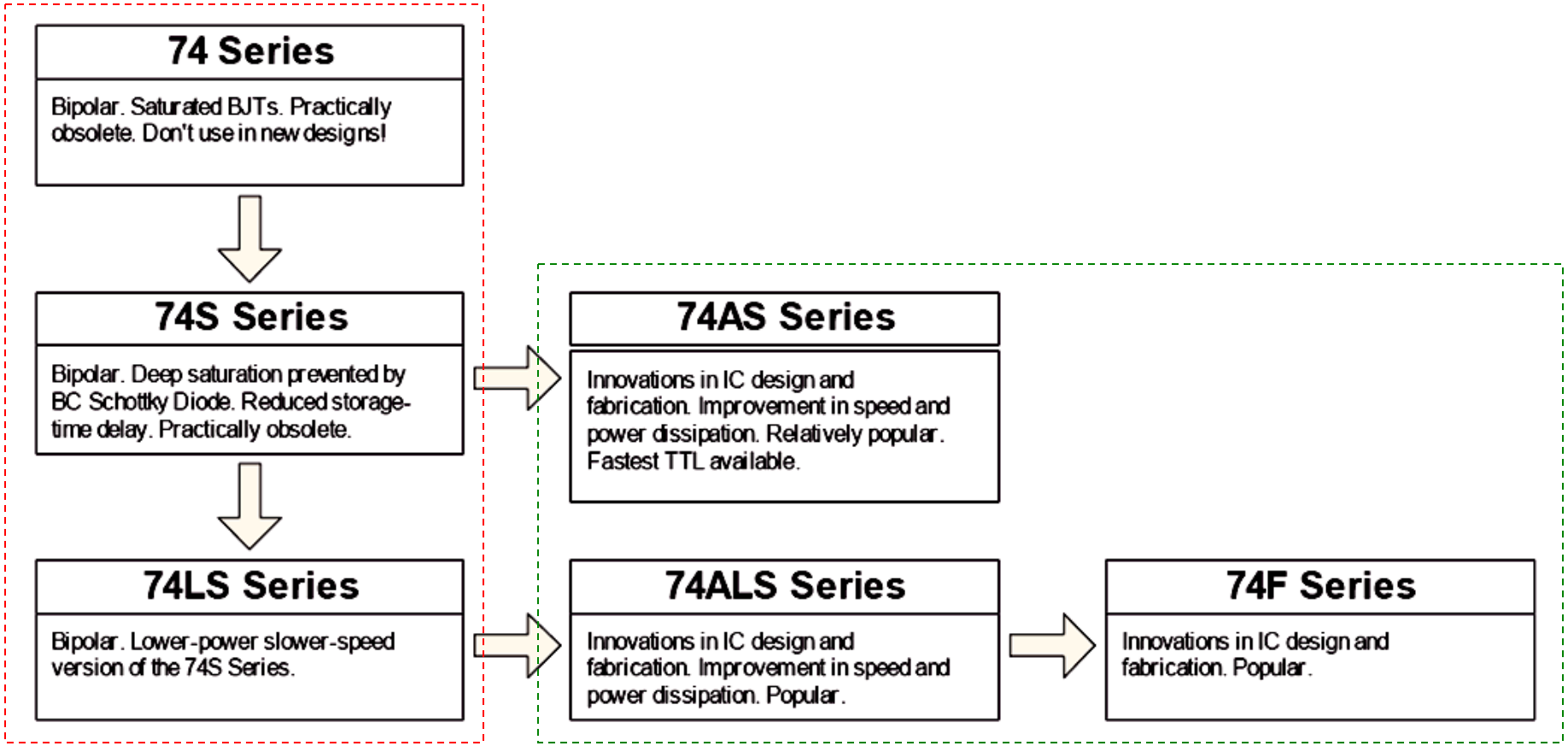
• A major slowdown factor in BJTs is due to transistors going in/out of saturation

• Shottky diode has a lower forward bias (0.25V)

• When BC junction would become forward biased, the Schottky diode bypasses the current preventing the transistor from going into saturation



TTL family evolution



Legacy: don't use in new designs

Widely used today

ECL

Emitter-Coupled Logic (ECL)

- PROS: Fastest logic family available (~1ns)
- CONS: low noise margin and high power dissipation
- Operated in emitter coupled geometry (recall differential amplifier or emitter-follower), transistors are biased and operate near their Q-point (never near saturation!)
- Logic levels. “0”: –1.7V. “1”: –0.8V
- Such strange logic levels require extra effort when interfacing to TTL/CMOS logic families.
- Open LTspice example: ECL inverter…

CMOS

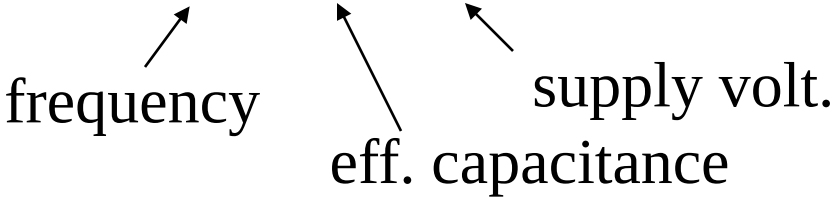
Complimentary MOS (CMOS)

- Other variants: NMOS, PMOS (obsolete)
- Very low static power consumption
- Scaling capabilities (large integration all MOS)
- Full swing: rail-to-rail output
- Things to watch out for:
  - don't leave inputs floating (in TTL these will float to HI, in CMOS you get undefined behaviour)
  - susceptible to electrostatic damage (finger of death)
- Open LTspice example: CMOS NOT and NAND…

CMOS/TTL power requirements

• TTL power essentially constant (no frequency dependence)

• CMOS power scales as $\propto f \times C \times V^2$



• At high frequencies (>> MHz) CMOS dissipates more power than TTL

• Overall advantage is still for CMOS even for very fast chips – only a relatively small portion of complicated circuitry operates at highest frequencies

CMOS family evolution

obsolete

4000 Series

CMOS. Wide supply voltage range. High noise margin. Low speed. Weak output drive. Practically obsolete.

74C Series

CMOS. Pin-compatible with TTL devices. Low speed. Obsolete. Replaced by HC/HCT family.

74HC/HCT Series

CMOS. Drastic increase in speed. Higher output drive capability. HCT input voltage levels compatible with TTL.

74AC/ACT Series

CMOS. Functionally compatible, but not pin-compatible to TTL. Improved noise immunity and speed. ACT inputs are TTL compatible.

74AHC/AHCT Series

CMOS. Improved speed, lower power, lower drive capability.

BiCMOS Logic

CMOS/Bipolar. Combine the best features of CMOS and bipolar. Low power high speed. Bus interfacing applications (74BCT, 74ABT)

74LVC/ALVC/LV/AVC

CMOS. Reduced supply voltage.
LVC: 5V/3.3V translation
ALVC: Fast 3.3V only
AVC: Optimised for 2.5V, down to 1.2V

General trend:

- Reduction of dynamic losses through successively decreasing supply voltages:
  $12V \rightarrow 5V \rightarrow 3.3V \rightarrow 2.5V \rightarrow 1.8V$
  CD4000 LVC/ALVC/AVC
- Power reduction is one of the keys to progressive growth of integration

Overview

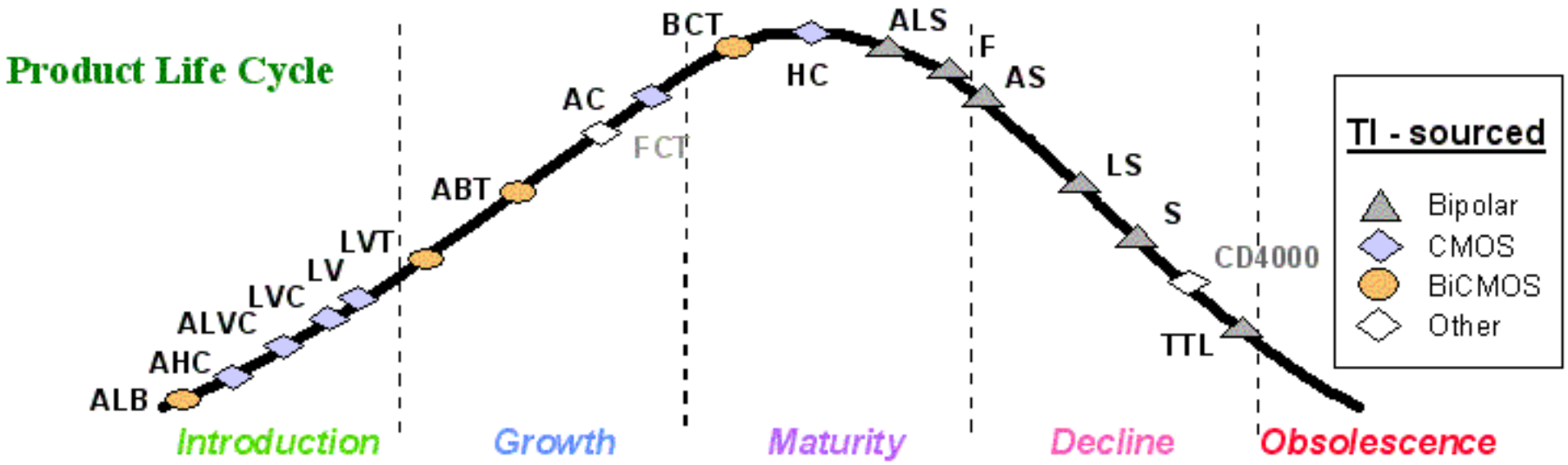
TTL

Logic Family	T_{PD}	$T_{rise/fall}$	$V_{IH,min}$	$V_{IL,max}$	$V_{OH,min}$	$V_{OL,max}$	Noise Margin
74	22ns		2.0V	0.8V	2.4V	0.4V	0.4V
74LS	15ns		2.0V	0.8V	2.7V	0.5V	0.3V
74F	5ns	2.3ns	2.0V	0.8V	2.7V	0.5V	0.3V
74AS	4.5ns	1.5ns	2.0V	0.8V	2.7V	0.5V	0.3V
74ALS	11ns	2.3ns	2.0V	0.8V	2.5V	0.5V	0.3V
ECL	1.45ns	0.35ns	-1.165V	-1.475V	-1.025V	-1.610V	0.135V
4000	250ns	90ns	3.5V	1.5V	4.95V	0.05V	1.45V
74C	90ns		3.5V	1.5V	4.5V	0.5V	1V
74HC	18ns	3.6ns	3.5V	1.0V	4.9V	0.1V	0.9V
74HCT	23ns	3.9ns	2.0V	0.8V	4.9V	0.1V	0.7V
74AC	9ns	1.5ns	3.5V	1.5V	4.9V	0.1V	1.4V
74ACT	9ns	1.5ns	2.0V	0.8V	4.9V	0.1V	0.7V
74AHC	3.7ns		3.85V	1.65V	4.4V	0.44V	0.55V

CMOS

- Values typical for $V_{cc}/V_{dd} = 5V$
- When interfacing different families, pay attention to their input/output voltage, current (fanout) specs.

Life-cycle


Product Life Cycle
ALB
AHC
ALVC
LVC
LV
LVT
ABT
AC
FCT
BCT
HC
ALS
F
AS
LS
S
CD4000
TTL
Introduction
Growth
Maturity
Decline
Obsolescence
TI - sourced
Bipolar
CMOS
BiCMOS
Other