Digital Logic Families
Overview

• Integration, Moore’s law
• Early families (DL, RTL)
• TTL
• Evolution of TTL family
• ECL
• CMOS family and its evolution
• Overview
Integration Levels

• Gate/transistor ratio is roughly 1/10
  – SSI < 12 gates/chip
  – MSI < 100 gates/chip
  – LSI …1K gates/chip
  – VLSI …10K gates/chip
  – ULSI …100K gates/chip
  – GSI …1Meg gates/chip
Moore’s law

• A prediction made by Moore (a co-founder of Intel) in 1965: “… a number of transistors to double every 2 years.”
In the beginning…

**Diode Logic (DL)**
- simplest; does not scale
- NOT not possible (need an active element)

**Resistor-Transistor Logic (RTL)**
- replace diode switch with a transistor switch
- can be cascaded
- large power draw
was...

Diode-Transistor Logic (DTL)
- essentially diode logic with transistor amplification
- reduced power consumption
- faster than RTL

DL AND gate

Saturating inverter
Logic families: V levels

$V_{OH}(\text{min})$ – The minimum voltage level at an output in the logical “1” state under defined load conditions

$V_{OL}(\text{max})$ – The maximum voltage level at an output in the logical “0” state under defined load conditions

$V_{IH}(\text{min})$ – The minimum voltage required at an input to be recognized as “1” logical state

$V_{IL}(\text{max})$ – The maximum voltage required at an input that still will be recognized as “0” logical state
Logic families: I requirements

$IOH$ – Current flowing into an output in the logical “1” state under specified load conditions

$I_{OL}$ – Current flowing into an output in the logical “0” state under specified load conditions

$I_{IH}$ – Current flowing into an input when a specified HI level is applied to that input

$I_{IL}$ – Current flowing into an input when a specified LO level is applied to that input
Logic families: fanout

Fanout: the maximum number of logic inputs (of the same logic family) that an output can drive reliably

\[ \text{DC fanout} = \min \left( \frac{I_{OH}}{I_{IH}}, \frac{I_{OL}}{I_{IL}} \right) \]
Logic families: propagation delay

$T_{PD,HL}$ – input-to-output propagation delay from HI to LO output

$T_{PD,LH}$ – input-to-output propagation delay from LO to HI output

Speed-power product: $T_{PD} \times P_{avg}$
Logic families: noise margin

HI state noise margin:
\[ V_{NH} = V_{OH}(\text{min}) - V_{IH}(\text{min}) \]

LO state noise margin:
\[ V_{NL} = V_{IL}(\text{max}) - V_{OL}(\text{max}) \]

Noise margin:
\[ V_N = \min(V_{NH}, V_{NL}) \]
Bipolar Transistor-Transistor Logic (TTL)
• first introduced by in 1964 (Texas Instruments)
• TTL has shaped digital technology in many ways
• Standard TTL family (e.g. 7400) is obsolete
• Newer TTL families still used (e.g. 74ALS00)

Distinct features
• Multi-emitter transistors
• Totem-pole transistor arrangement
• Open LTspice example: TTL NAND...
TTL evolution

Schottky series (74LS00) TTL

• A major slowdown factor in BJTs is due to transistors going in/out of saturation
• Shottky diode has a lower forward bias (0.25V)
• When BC junction would become forward biased, the Shottky diode bypasses the current preventing the transistor from going into saturation
TTL family evolution

**74 Series**
- Bipolar. Saturated BJTs. Practically obsolete. Don’t use in new designs!

**74S Series**

**74LS Series**
- Bipolar. Lower-power slower-speed version of the 74S Series.

**74AS Series**
- Innovations in IC design and fabrication. Improvement in speed and power dissipation. Relatively popular. Fastest TTL available.

**74ALS Series**
- Innovations in IC design and fabrication. Improvement in speed and power dissipation. Popular.

**74F Series**
- Innovations in IC design and fabrication. Popular.

Legacy: don’t use in new designs

Widely used today
ECL

Emitter-Coupled Logic (ECL)
• **PROS**: Fastest logic family available (~1ns)
• **CONS**: low noise margin and high power dissipation
• Operated in emitter coupled geometry (recall differential amplifier or emitter-follower), transistors are biased and operate near their Q-point (never near saturation!)
• Logic levels. “0”: –1.7V. “1”: –0.8V
• Such strange logic levels require extra effort when interfacing to TTL/CMOS logic families.
• **Open LTspice example: ECL inverter…**
CMOS

Complimentary MOS (CMOS)

• Other variants: NMOS, PMOS (obsolete)
• Very low static power consumption
• Scaling capabilities (large integration all MOS)
• Full swing: rail-to-rail output

Things to watch out for:
– don’t leave inputs floating (in TTL these will float to HI, in CMOS you get undefined behaviour)
– susceptible to electrostatic damage (finger of death)

• Open LTspice example: CMOS NOT and NAND…
CMOS/TTL power requirements

• TTL power essentially constant (no frequency dependence)
• CMOS power scales as \( \propto f \times C \times V^2 \)

- frequency
- supply volt.
- eff. capacitance

• At high frequencies (>> MHz) CMOS dissipates more power than TTL
• Overall advantage is still for CMOS even for very fast chips – only a relatively small portion of complicated circuitry operates at highest frequencies
CMOS family evolution

General trend:
- Reduction of dynamic losses through successively decreasing supply voltages:
  \[12V \rightarrow 5V \rightarrow 3.3V \rightarrow 2.5V \rightarrow 1.8V\]

CD4000 LVC/ALVC/AVC
- Power reduction is one of the keys to progressive growth of integration

<table>
<thead>
<tr>
<th>4000 Series</th>
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<tr>
<th>74C Series</th>
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<tr>
<th>74HC/HCT Series</th>
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</thead>
<tbody>
<tr>
<td>CMOS. Drastic increase in speed. Higher output drive capability. HCT input voltage levels compatible with TTL.</td>
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<table>
<thead>
<tr>
<th>74AC/ACT Series</th>
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</thead>
<tbody>
<tr>
<td>CMOS. Functionally compatible, but not pin-compatible to TTL. Improved noise immunity and speed. ACT inputs are TTL compatible.</td>
</tr>
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<thead>
<tr>
<th>74AHC/AHCT Series</th>
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<tbody>
<tr>
<td>CMOS. Improved speed, lower power, lower drive capability.</td>
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<tr>
<th>BiCMOS Logic</th>
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<tbody>
<tr>
<td>CMOS/Bipolar. Combine the best features of CMOS and bipolar. Low power high speed. Bus interfacing applications (74BCT, 74ABT)</td>
</tr>
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<thead>
<tr>
<th>74LVC/ALVC/LV/AVC</th>
</tr>
</thead>
<tbody>
<tr>
<td>CMOS. Reduced supply voltage. LVC: 5V/3.3V translation ALVC: Fast 3.3V only AVC: Optimised for 2.5V, down to 1.2V</td>
</tr>
</tbody>
</table>
### TTL

<table>
<thead>
<tr>
<th>Logic Family</th>
<th>$T_{PD}$</th>
<th>$T_{rise/fall}$</th>
<th>$V_{IH,min}$</th>
<th>$V_{IL,max}$</th>
<th>$V_{OH,min}$</th>
<th>$V_{OL,max}$</th>
<th>Noise Margin</th>
</tr>
</thead>
<tbody>
<tr>
<td>74</td>
<td>22ns</td>
<td>2.0V</td>
<td>0.8V</td>
<td>2.4V</td>
<td>0.4V</td>
<td>0.4V</td>
<td>0.4V</td>
</tr>
<tr>
<td>74LS</td>
<td>15ns</td>
<td>2.0V</td>
<td>0.8V</td>
<td>2.7V</td>
<td>0.5V</td>
<td>0.3V</td>
<td></td>
</tr>
<tr>
<td>74F</td>
<td>5ns</td>
<td>2.3ns</td>
<td>2.0V</td>
<td>0.8V</td>
<td>2.7V</td>
<td>0.5V</td>
<td>0.3V</td>
</tr>
<tr>
<td>74AS</td>
<td>4.5ns</td>
<td>1.5ns</td>
<td>2.0V</td>
<td>0.8V</td>
<td>2.7V</td>
<td>0.5V</td>
<td>0.3V</td>
</tr>
<tr>
<td>74ALS</td>
<td>11ns</td>
<td>2.3ns</td>
<td>2.0V</td>
<td>0.8V</td>
<td>2.5V</td>
<td>0.5V</td>
<td>0.3V</td>
</tr>
<tr>
<td>ECL</td>
<td>1.45ns</td>
<td>0.35ns</td>
<td>-1.165V</td>
<td>-1.475V</td>
<td>-1.025V</td>
<td>-1.610V</td>
<td>0.135V</td>
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<tr>
<td>4000</td>
<td>250ns</td>
<td>90ns</td>
<td>3.5V</td>
<td>1.5V</td>
<td>4.95V</td>
<td>0.05V</td>
<td>1.45V</td>
</tr>
<tr>
<td>74C</td>
<td>90ns</td>
<td>3.5V</td>
<td>1.5V</td>
<td>4.5V</td>
<td>0.5V</td>
<td>1V</td>
<td></td>
</tr>
<tr>
<td>74HC</td>
<td>18ns</td>
<td>3.6ns</td>
<td>3.5V</td>
<td>1.0V</td>
<td>4.9V</td>
<td>0.1V</td>
<td>0.9V</td>
</tr>
<tr>
<td>74HCT</td>
<td>23ns</td>
<td>3.9ns</td>
<td>2.0V</td>
<td>0.8V</td>
<td>4.9V</td>
<td>0.1V</td>
<td>0.7V</td>
</tr>
<tr>
<td>74AC</td>
<td>9ns</td>
<td>1.5ns</td>
<td>3.5V</td>
<td>1.5V</td>
<td>4.9V</td>
<td>0.1V</td>
<td>1.4V</td>
</tr>
<tr>
<td>74ACT</td>
<td>9ns</td>
<td>1.5ns</td>
<td>2.0V</td>
<td>0.8V</td>
<td>4.9V</td>
<td>0.1V</td>
<td>0.7V</td>
</tr>
<tr>
<td>74AHC</td>
<td>3.7ns</td>
<td>3.85V</td>
<td>1.65V</td>
<td>4.4V</td>
<td>0.44V</td>
<td>0.55V</td>
<td></td>
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</tbody>
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- Values typical for $V_{cc}/V_{dd} = 5V$
- When interfacing different families, pay attention to their input/output voltage, current (fanout) specs.
Life-cycle