A/D and D/A converters
- most physical variables are analog
- humans respond most efficiently to data represented in analog form
  ⇒ must perform A/D & D/A conversion to utilize computers & digital circuitry

Digital representation of info (time varying)
- sampling time $T_s = \frac{1}{f_s}$
- use n-bit binary representation of a variable

- both sampling time and # of bits affect fidelity of representation
1) # bits - precision (smallest variation that can be still represented)

E.g. 10V p-p signal, \( n = 10 \) bits

\[
\Delta V_{\text{min}} = \frac{V_{\text{range}}}{2^n - 1} \approx 10\text{mV} \quad \text{(if using the full range of D/A or A/D converter)}
\]

2) Sampling rate \( f_s = \frac{1}{T_s} \) determines the highest freq. content (actually \( f_s/2 \)) < sampling theorem

D/A Conversion

\[
\text{VALUE} = 2^{n-1}B_{n-1} + \ldots + 2^0B_0
\]

Recall summing circuit

\[
\text{Sout} = -R_F I_F \quad \text{logic volt. levels (0-5V)}
\]

\[
\text{Sout} = -\left(\frac{R_F}{R_{n-1}}B_{n-1} + \ldots + \frac{R_F}{R_0}B_0\right)
\]

Assume \( R_0 = R, R_1 = \frac{R}{2}, \ldots \)

\[
\text{Sout} = -\frac{R_F}{R_0} \left(2^{n-1}B_{n-1} + \ldots + 2^0B_0\right)
\]
Problems

1) $R$'s must be very accurate
   
   e.g. 16-bit $\sim \pm 0.0015\% \left( \frac{R_F}{R_{n-1}} \right)$ accuracy

2) large range of $R$'s

3) $B_{n-1}, ..., B_0$ must be just as accurate

R-2R ladder D/A converter (DAC)
starting from LSB
digital "0" or "1"
a) \[ V_{\text{ref} \cdot b_0} \]  
\[ \frac{2R}{2R} \]  
\[ \frac{2R}{2R} \]  
\[ \frac{1}{2} V_{\text{ref} \cdot b_0} \]  
\[ \frac{1}{4} V_{\text{ref} \cdot b_0} \]  
\[ R \]  
\[ R \]  
\[ \frac{1}{2} V_{\text{ref} \cdot b_0} \]  
\[ \frac{1}{4} V_{\text{ref} \cdot b_0} \]  

b) \[ \frac{2R}{2R} \]  
\[ \frac{2R}{2R} \]  
\[ \frac{1}{2} V_{\text{ref} \cdot b_0} \]  
\[ \frac{1}{4} V_{\text{ref} \cdot b_0} \]  
\[ R \]  
\[ R \]  
\[ \frac{1}{2} V_{\text{ref} \cdot b_0} \]  
\[ \frac{1}{4} V_{\text{ref} \cdot b_0} \]  

c) etc.: Thev. resistance is always \( R \)  
Thev. voltage \( \Rightarrow \frac{1}{2} \) for each stage

e.g. for 4-bits

\[ \frac{1}{2^4} V_{\text{ref} \cdot b_0} \]  
\[ R \]  
\[ R \]  
\[ V_{\text{out}} \]  

"Activate" each bit by superposition to get

\[ V_{\text{out}} = -\frac{R_F}{2^n R} V_{\text{ref}} \left( 2^{n-1} b_{n-1} + \ldots + 2^0 b_0 \right) \]

n-bit DAC

- widely used
- (another widely used type ΣΔ modulator, next week)