DAC specifications
- bit resolution
- accuracy
- linearity
- settling time

ADC (A/D Converters)

staircase:
problems with staircase:

b) susceptible to noise

successive approximation ADC

bits are set starting from _____

1)
2)
3)
4)

Ex. 3-bit ADC, 0-7V
\( V_m = 2.5V \)
good:

bad:

Flash ADC
- resistor ladder
- input $V_{in}$
- ______ encoder

good:

bad:

Integrating ADC
Dual slope ADC
1) \[ S_1 = \]

2) slope \( \propto \) input voltage

good:

bad:
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**Σ-Δ modulator**

- **Σ-Δ name**
- unlike other ADC types,
- negative feedback theory:
- (parallel) binary output is obtained

Refer to the schematic
- op-amp #1
- op-amp #2
- op-amp #3
Nyquist sampling criterion & aliasing

- if

- if

- if

signal with freq. f

measured freq.

actual freq.
Effect of conversion time ($t_c$) on resolution

$$V_m = V_0 \sin (2\pi ft)$$

$$V_{p-p} = 2V_0$$

E.g. 8-bit ADC with $t_c = 10\,\mu s$ (100kHz)
Sample & hold circuit

General A/D converter layout

Digital scopes
   Sampling

Real-time
Electrical Noise

Signal to noise ratio

\[ \text{SNR}_{\text{dB}} = \]

Noise figure

\[ \text{NF}_{\text{dB}} = \]

E.g. 1dB noise figure:
Sources of Noise

I. Intrinsic
II. Interference

Intrinsic sources of noise

1) Johnson (thermal) noise

\[(V_n)_{rms} = \]
- "white noise"

- "gaussian noise"

Ex: $R=20\,k\Omega \at T=300K, B=20kHz$

2) Shot noise

Ex: $\dot{I}_S=1A, B=20kHz$
$\dot{I}_S=10\,pA$

- also

3) $1/f$ (flicker) noise
\[ \log \left( \frac{dp}{dt} \right) \]

\[ \log f \]

- a.k.a.

To minimize intrinsic noise

- limit