

PHYS3360/AEP3630

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Lecture 37

DAC specifications

- bit resolution
- accuracy
- linearity
- settling time

ADC (A/D converters)

staircase:

problems with staircase :

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b) susceptible to noise

successive approximation ADC

bits are set starting from \_\_\_\_\_

1)

2)

3)

4)

Ex 3-bit ADC , 0-7V  
 $V_m = 2.5V$

good:

bad:

Flash ADC

- resistor ladder

- input  $v_m$

- \_\_\_\_\_ encoder

good:

bad:

Integrating ADC

Dual slope ADC

1)

$$v_1 =$$

2)

slope  $\propto$  input voltage

good:

bad: