DAC specifications (same for ADC)

- bit resolution \( = \frac{\Delta V_{\text{max}}}{2^n - 1} \quad n = \# \text{ of bits} \)

- accuracy = deviation in the entire scale from specified value

- linearity = deviation of the output from best straight line fit

- settling time = time it takes for output to settle to within \( \pm \frac{1}{2} \text{LSB} \) of the value

**e.g. in the lab DAC 0808**

- \( n = 8 \) bits
- linearity = \( \pm 0.2\% \)
- settling time = 150ns (\( \sim 7\text{MHz} \))

ADC (A/D converters)  (see the printout)

**staircase**: value in counter after it is stopped

\( \alpha \ x \sin \) (uses D/A converter)
problems with staircase:

a) time to convert varies
   \[ t_c \leq 2^n \Delta t \]  
   (occasionally need to go thru full staircase)
   clock tick

b) susceptible to noise
not used in practice

successive approximation ADC
same as binary search algorithm
bits are set starting from MSB

1) begin by setting all bits to "0"
2) set MSB = 1 (DAC inside)
3) if \( V_{DAC} < \frac{1}{2} V_m \) leave MSB = 1
   otherwise MSB = 0
4) repeat 1-3 until all bits are set

Ex: 3-bit ADC, 0-7V
\( V_m = 2.5V \)

<table>
<thead>
<tr>
<th>DAC bits before</th>
<th>( V_{DAC} )</th>
<th>DAC bits after</th>
</tr>
</thead>
<tbody>
<tr>
<td>100</td>
<td>4V</td>
<td>000</td>
</tr>
<tr>
<td>010</td>
<td>2V</td>
<td>010</td>
</tr>
<tr>
<td>011</td>
<td>3V</td>
<td>010</td>
</tr>
</tbody>
</table>
good: faster than staircase fixed conversion time not clock tick

bad: still susceptible to noise

Flash ADC
- resistor ladder divides Vref into $2^n-1$ identical segments
- input signal simultaneously compared with each segment

- priority encoder provides binary output

good: fast (<10ns conversion time)
bad: need $2^n-1$ comparators (large #)

- e.g. 8-bit = 255
- 12-bit = 4095

(typically limited to 8-bit ADC)

Integrating ADC - much better noise immunity
Dual slope ADC - built-in averaging

2 step process
1) a) counter is reset; $S_1$ closed; cap discharged
   b) $S_1$ open; $S_2$ connected to $V_{in}$
   c) integrate $V_{in}$ for $T_{fixed} = m \Delta t$ (clock tick)

   $\Delta S_1 = -\frac{1}{RC} \int V_{in} dt = -\frac{T_{fixed}}{RC} \langle V_{in} \rangle$

   avg. over m CR time

2) a) $S_2$ now connected to $-V_{ref}$, counter starts counting
   b) when $\Delta S_1$ integrates back to 0, stop the clock

slope $\propto$ input voltage ($V_{in}$ or $-V_{ref}$)

when will clock stop?

   $-\frac{m \Delta t}{RC} \langle V_{in} \rangle = \frac{e \Delta t}{RC} (-V_{ref})$

   $\langle V_{in} \rangle = \frac{e}{m} V_{ref}$

   $\Delta S_1$ (step 2)

   $\Delta S_1 = -\frac{T_{fixed}}{RC} \langle V_{in} \rangle$

   $\langle V_{in} \rangle = \frac{e}{m} V_{ref}$

   $\Delta S_1$ (step 1)

good: noise (spike in volt.) immunity (integrator)
   accuracy indep. of $R, C, \Delta t$ values
   most commonly used (DVM - digital volt. meters)

bad: slow, conversion time $\sim (m+e) \Delta t$