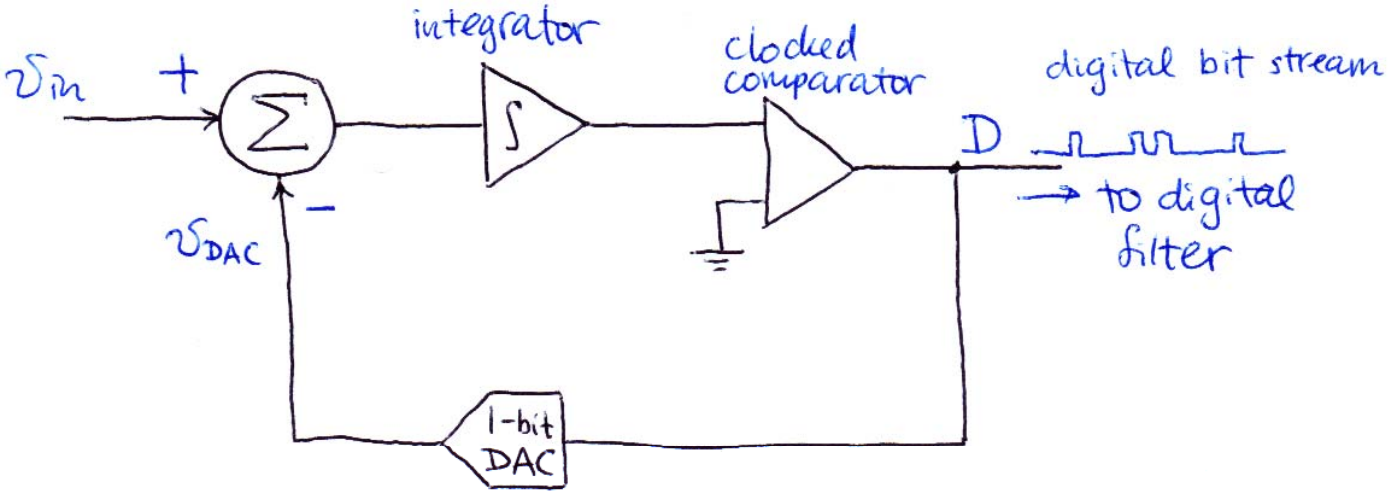
Lecture 38

Σ-Δ modulator (ADC)



- Σ-Δ name comes from adding (Σ) v_{in} and subtracting 1-bit DAC output (Δ) v_{DAC}
- unlike other ADC types, Σ-Δ is closed loop config.
- negative feedback theory: $\langle v_{DAC} \rangle \rightarrow v_{in}$
- (parallel) binary output is obtained by averaging the serial bit stream (e.g. use counter to collect the total # of 1's over a fixed # of clock ticks)

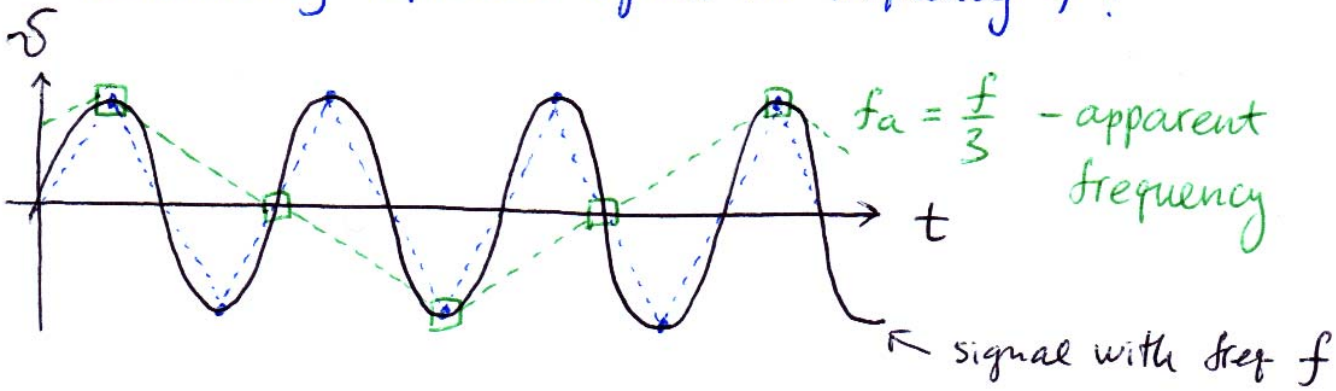
Refer to the schematic (the printout)

- op-amp #1 : summing integrator (v_{in} subtracted, => inversed bit stream)
- op-amp #2 : 1-bit ADC
- op-amp #3 : shift 0/5 V to −V/+V signal

Ex. integrator output is high, $v_{DAC} = +V$, pulls the integ. low until $\langle v_{DAC} \rangle \rightarrow -v_{in}$ see trace examples / LTspice

Nyquist sampling criterion & aliasing

Q: basic question – what must the sampling rate be to accurately represent signal at frequency f?



- $f_s = 2f \quad (= \frac{1}{t_s})$

□ $f_s = \frac{4}{3}f$

– if $f_s > 2f$, no aliasing occurs

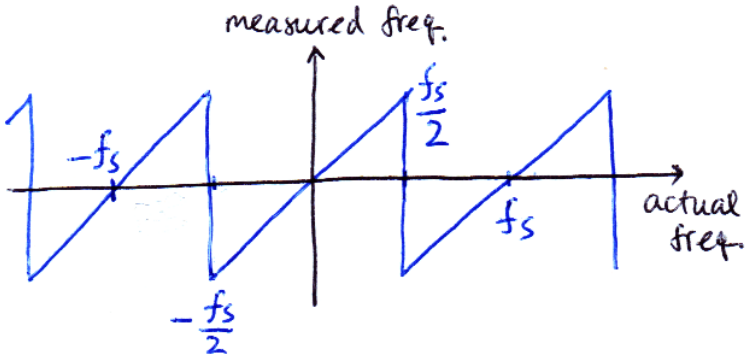
⇒ Nyquist theorem: choose $f_s > 2f_{max}$

highest freq. in the signal

– if $f < f_s < 2f$, aliasing

$f_a = f_s - f$

– if $f_s < f$, aliasing $f_a = f_s - f \,(\text{mod } f_s)$



Q: how to avoid aliasing?

A: use LP filter $< \frac{f_s}{2}$

Effect of conversion time (t_c) on resolution

$v_{in} = v_0 \sin(2\pi f t)$ ← digitize with n-bit resolution

What is the largest f for v_{in} to change less than 1LSB in time t_c?

$V_{p-p} = 2v_0$, resolution $\frac{V_{p-p}}{2^n - 1} = \Delta v_r$

$$\Delta v_r = \left.\frac{dv_{in}(t)}{dt}\right|_{max} t_c = 2\pi f v_0 t_c \;, \Rightarrow$$

$$\boxed{f \leq \frac{1}{\pi}\,\frac{1}{2^n - 1}\,\frac{1}{t_c}}$$ otherwise, the resolution is lost

E.g. 8-bit ADC with $t_c = 10\mu s$ (100kHz)

⇒ will digitize to 8-bit accuracy only if

$f \leq 125$ Hz (not 100kHz!)

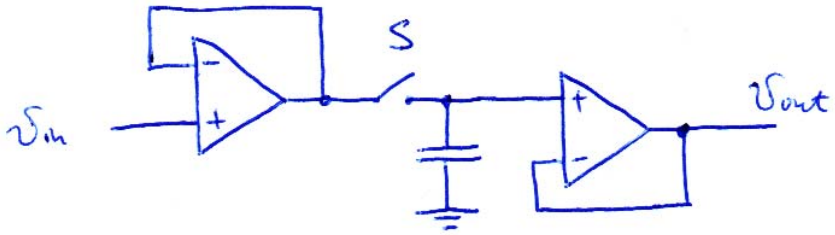
Effective resolution can be substantially worse than bit resolution for fast signals

- there may be no sense in choosing higher-bit ADC for a given f / t_c combination

Q: newest scopes can digitize at 20 GHz (~50ps). How? No ADC is that fast!

Sample & hold circuit (see the printout)

– use "fast memory" to record the trace, digitize later



S is hi-speed FET switch

V_{out} holds V_c after S is opened

General A/D converter layout (see the printout)

Digital scopes

Sampling

– 100 GHz BW doable

– very high BW is achieved via reconst. of repetitive signal on multiple passes with variable delay

Real-time

– max BW 20 GHz (typically < 1 GHz)

– acquire the whole trace in a single shot using sample & hold; then A/D convert