**Σ-Δ modulator (ADC)**

- Σ-Δ name comes from adding (Σ) $V_{in}$ and subtracting 1-bit DAC output (Δ) $V_{DAC}$
- Unlike other ADC types, Σ-Δ is closed loop config.
- Negative feedback theory: $\langle V_{DAC} \rangle \rightarrow V_{in}$
- (Parallel) binary output is obtained by averaging the serial bit stream (e.g., use counter to collect the total # of 1's over a fixed # of clock ticks)

Refer to the schematic (the printout)
- Op-amp #1: Summing integrator ($V_{in}$ subtracted, $\Rightarrow$ Inverted bit stream)
- Op-amp #2: 1-bit ADC
- Op-amp #3: Shift 0/5V to -V/+V signal

Ex. Integrator output is high, $V_{DAC} = +V$, pulls the integrator low until $\langle V_{DAC} \rangle \rightarrow -V_{in}$, see trace examples/LTSpice
Nyquist sampling criterion & aliasing

Q: basic question - what must the sampling rate be to accurately represent signal at frequency \( f \)?

\[ f_s = 2f \quad (= \frac{1}{t_s}) \]

\[ f_s = \frac{4}{3} f \]

- if \( f_s > 2f \), no aliasing occurs
  \[ \Rightarrow \text{Nyquist theorem: choose } f_s > 2f_{\text{max}} \]
  \( \text{highest freq. in the signal} \)

- if \( f < f_s < 2f \), aliasing
  \[ f_a = f_s - f \]

- if \( f_s < f \), aliasing
  \[ f_a = f_s - f \ (\text{mod } f_s) \]

Q: how to avoid aliasing?
A: use LP filter \(< \frac{f_s}{2}\)
Effect of conversion time (tc) on resolution

\[ V_m = V_0 \sin (2\pi ft) \]  
\( \text{digitize with n-bit resolution} \)

What is the largest \( f \) for \( V_m \) to change less than 1LSB in time \( tc \)?

\[ V_{p-p} = 2V_0, \quad \text{resolution} \quad \frac{V_{p-p}}{2^n - 1} = \Delta V_r \]

\[ \Delta V_r = \left. \frac{dV_m(t)}{dt} \right|_{max} \cdot \text{tc} = 2\pi f V_0 \text{ tc}, \quad \Rightarrow \]

\[ f \leq \frac{1}{\pi} \frac{1}{2^n - 1} \frac{1}{\text{tc}} \]

otherwise, the resolution is lost

E.g. 8-bit ADC with \( \text{tc} = 10 \mu s \) (100kHz)

\[ \Rightarrow \text{will digitize to 8-bit accuracy only if} \]

\[ f \leq 125 \text{ Hz} \quad (\text{not} \ 100\text{kHz}) \]

**Effective resolution** can be substantially worse than bit resolution for fast signals

- there may be no sense in choosing higher-bit ADC for a given \( f / \text{tc} \) combination

Q: newest scopes can digitize at 20GHz (~50ps). How?

No ADC is that fast!
Sample & hold circuit (see the printout)
- use "fast memory" to record the trace, digitize later

\[ S_m \quad \text{to} \quad \text{Out} \]

S is hi-speed FET switch
Out holds Vc after
S is opened

General A/D converter layout (see the printout)

Digital scopes

Sampling
- 100GHz BW doable
- very high BW is achieved
  via reconst. of repetitive signal on multiple passes
  with variable delay

Real-time
- max BW 20GHz
  (typically < 1GHz)
- acquire the whole trace in a single shot using sample & hold; then A/D convert