	J21 (Backplane from Mainframe)	To Module DIN96 Pin#	Name on 1469 Schematic	Description
1	AC_FAIL_COLL			
2	CFG0	A21	CONFIG0	Selects Mode, Active During Reset XILINX, Pin 77
3	INH_24V_ACTIVE_LOW			
4	CFG1	A23	CONFIG1	U29 EEPROM Write Enable, U29 Pin 27 Xilinx Pin 78
5	GLOBAL_INHIBIT			
6	CFG2	A25	CONFIG2	Xilinx Pin 79
7	PWAGND			
8	CFG3	A27	CONFIG3	Xilinx Pin 80
9	GA4	A5	GA4	Xilinx Pin 7
10	CFG4	C21	CONFIG4	Xilinx Pin 81
11	GA45	A6	GA5	Xilinx Pin 8
12	CFG5	C23	CONFIG5	Xiinx Pin 82
13	GA6	A7	GA6	Xilinx Pin 9
14	CFG6	C25	CONFIG6	Xiinx Pin 83
15	GA7	A8	GA7	Xilinx Pin 10
16	CFG7	C27	CONFIG7	Xilinx Pin 84
17	8MHz	A10	CONTROL0	68HC11 Clock & XILINX (U20) Clock
18	24V_GOOD			
19	MISO	A12 (Module Serial Out?)	CONTROL1	68HC11 PO0, PIN 43, TXD
20	GND			
21	MOSI	A14 (Module Serial Input?)	CONTROL2	68HC11 PO0, PIN 42, RXD
22	GND			
23	ATTN*	C1	CONTROL3	68HC11 PA6, PIN 2, Output
24	GND			
25	HV_ENABLE*	C3	CONTROL4	68HC11 PA1, PIN 7
26	GND			
27	100KHZ	C5	CONTROL5	Input to FPGA U3, Pin 2 Xilinx Pin 67
28	GND			
29	800KHZ	C7	CONTROL6	Clock for PGA U3, Pin 1 Xilinx Pin 13
30	GND			
31	SYSRESET	C12	CONTROL7	U10 F08 (AND) Pin 12
32	GND			
33	20MHZ	C14	CONTROL8	
34	GND			
35	ARCNET	C16	CONTROL9	
36	GND			
37	UCLK	C18	CONTROL10	
38	GND			